



BUK9Q39-100L

100 V, 39 mOhm logic level N-channel MOSFET in MLPAK33

10 December 2025

Product data sheet

1. General description

Logic level N-channel MOSFET in a small MLPAK33-WF package using Trench12 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Logic-level compatible
- Trench12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Automotive qualified to AEC-Q101 at 175°C
- Side-wettable flanks for robust solder joints and automatic optical inspection

3. Applications

- LED lighting
- DC-to-DC conversion
- Solenoid, motor and other load switching
- Circuit protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	19	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	29	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 4.8\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		-	32	39.5	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 4.8\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14		-	1.5	-	nC

[1] 19 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33-WF (SOT8002-3)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Q39-100L	MLPAK33-WF	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Q39-100L	8AW

8. Limiting values

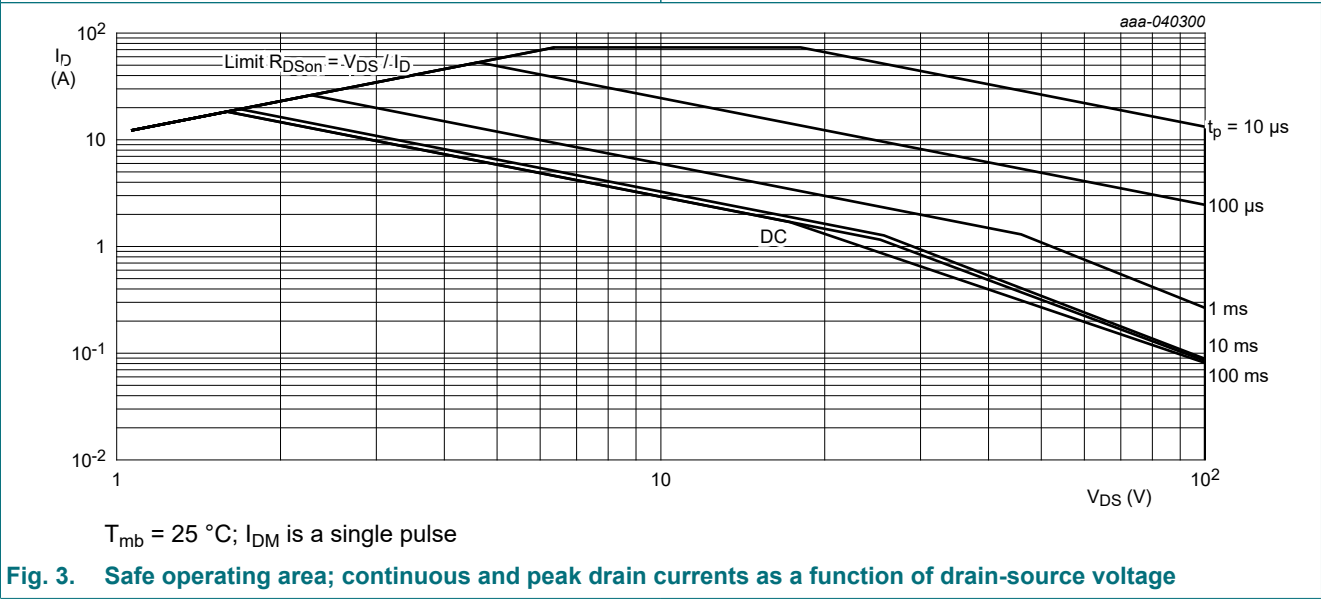
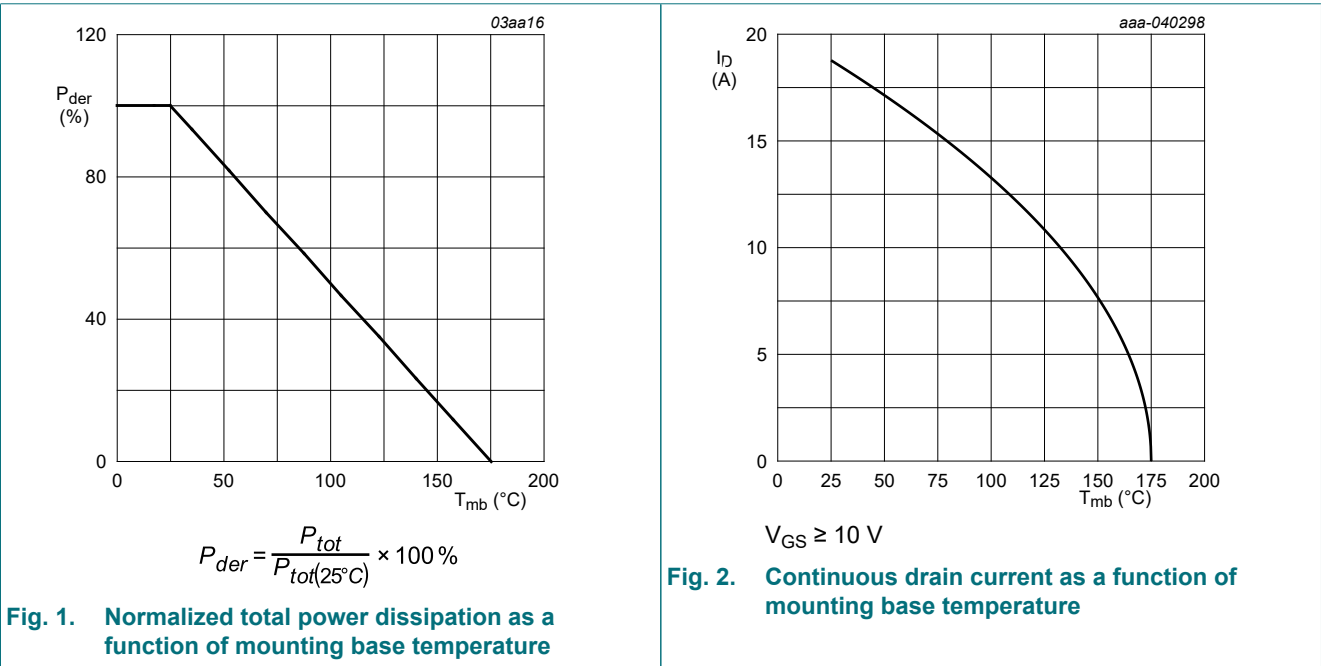
Table 5. Limiting values

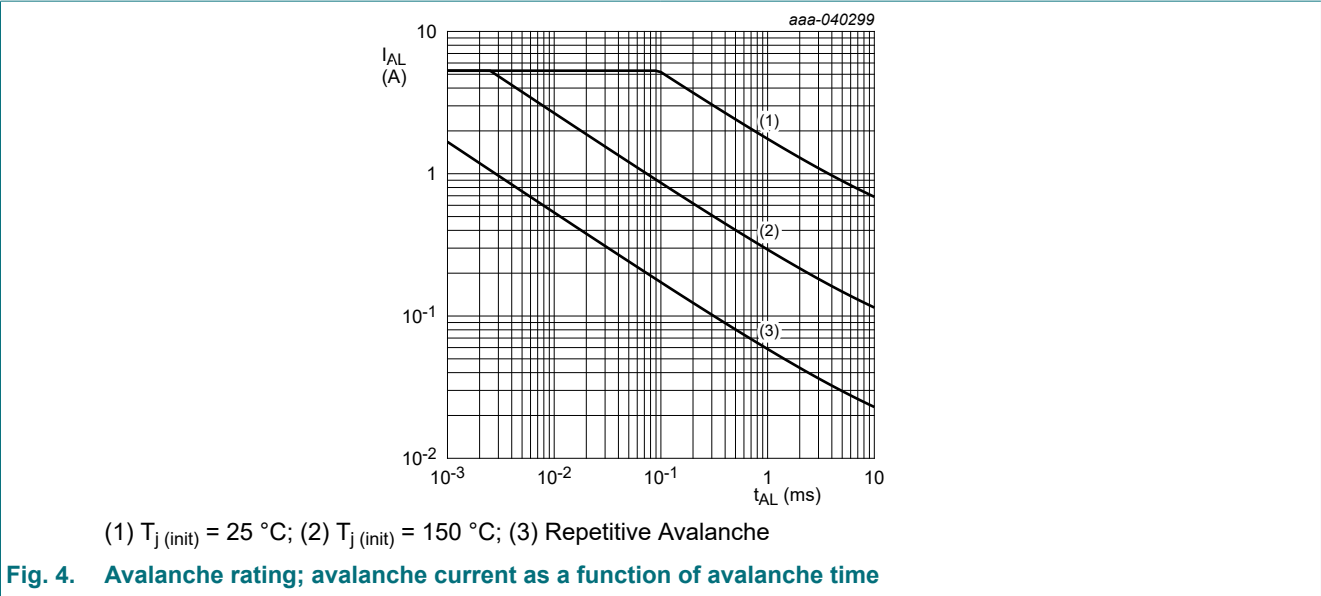
In accordance with the Absolute Maximum Rating System (IEC 60134). *T*_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ <i>T</i> _j ≤ 175 °C		-	100	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	<i>T</i> _{mb} = 25 °C; Fig. 1		-	29	W
<i>I</i> _D	drain current	V _{GS} = 10 V; <i>T</i> _{mb} = 25 °C; Fig. 2	[1]	-	19	A
		V _{GS} = 10 V; <i>T</i> _{mb} = 100 °C; Fig. 2		-	13	A
<i>I</i> _{DM}	peak drain current	pulsed; <i>t</i> _p ≤ 10 μs; <i>T</i> _{mb} = 25 °C; Fig. 3		-	75	A
<i>T</i> _{stg}	storage temperature			-55	175	°C
<i>T</i> _j	junction temperature			-55	175	°C
Source-drain diode						
<i>I</i> _S	source current	<i>T</i> _{mb} = 25 °C		-	19	A
<i>I</i> _{SM}	peak source current	pulsed; <i>t</i> _p ≤ 10 μs; <i>T</i> _{mb} = 25 °C		-	75	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 5.3\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{J(init)} = 25\text{ }^\circ\text{C}$; unclamped; $t_p = 95\text{ }\mu\text{s}$; Fig. 4	[2] [3]	-	32.8	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 100\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{J(init)} = 25\text{ }^\circ\text{C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[2] [3]	-	5.3	A

- [1] 19 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.



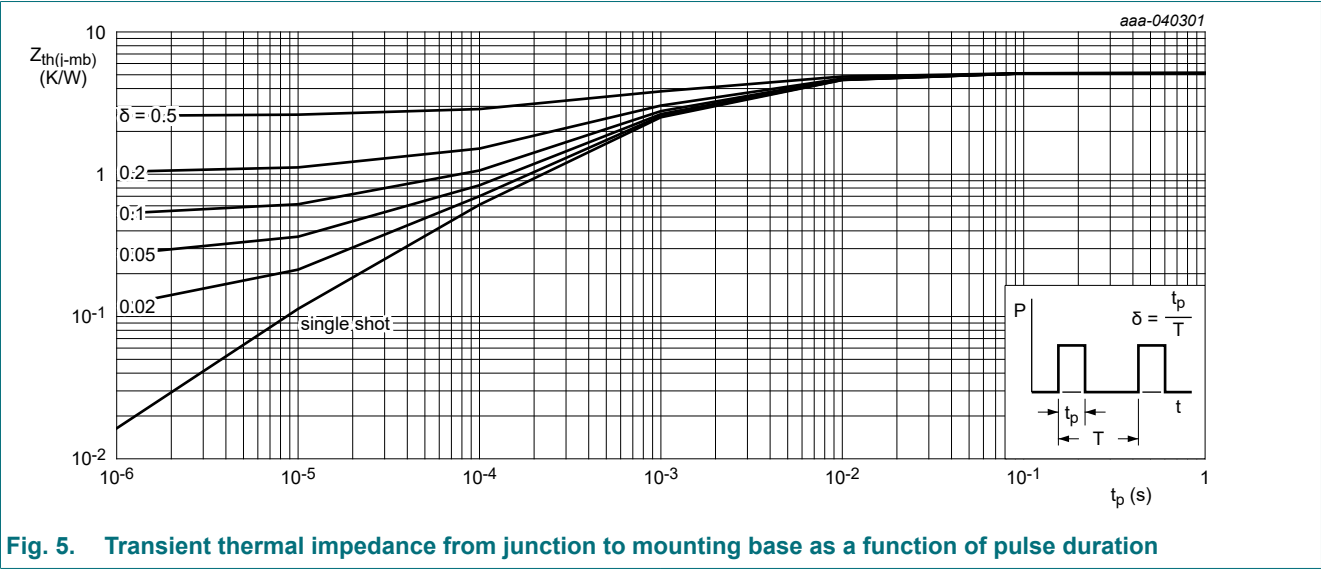


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	3.4	5.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	40	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$		100	115	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -40\ ^\circ C$		97	112	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -55\ ^\circ C$		96	111	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_j = 25\ ^\circ C$; Fig. 9 ; Fig. 10		1.45	1.7	2.15	V
I_{DSS}	drain leakage current	$V_{DS} = 100\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$		-	1	-	μA
		$V_{DS} = 100\ V$; $V_{GS} = 0\ V$; $T_j = 125\ ^\circ C$		-	20	-	μA
		$V_{DS} = 100\ V$; $V_{GS} = 0\ V$; $T_j = 175\ ^\circ C$		-	200	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$		-	100	-	nA
		$V_{GS} = -20\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$		-	-100	-	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 4.8\ A$; $T_j = 25\ ^\circ C$; Fig. 11		-	32	39.5	m Ω
		$V_{GS} = 10\ V$; $I_D = 4.8\ A$; $T_j = 105\ ^\circ C$; Fig. 12		-	49	64	m Ω
		$V_{GS} = 10\ V$; $I_D = 4.8\ A$; $T_j = 125\ ^\circ C$; Fig. 12		-	55	72	m Ω
		$V_{GS} = 10\ V$; $I_D = 4.8\ A$; $T_j = 175\ ^\circ C$; Fig. 12		-	69	83	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 3.9\ A$; $T_j = 25\ ^\circ C$; Fig. 11		-	40	59	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 3.9\ A$; $T_j = 105\ ^\circ C$; Fig. 12		-	61	86	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 3.9\ A$; $T_j = 125\ ^\circ C$; Fig. 12		-	67	95	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 3.9\ A$; $T_j = 175\ ^\circ C$; Fig. 12		-	84	124	m Ω
R_G	gate resistance	$f = 1\ MHz$; $T_j = 25\ ^\circ C$		-	1.2	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 4.8\ A$; $V_{DS} = 50\ V$; $V_{GS} = 10\ V$; $T_j = 25\ ^\circ C$; Fig. 13 ; Fig. 14		-	13.5	20	nC
		$I_D = 4.8\ A$; $V_{DS} = 50\ V$; $V_{GS} = 5\ V$; $T_j = 25\ ^\circ C$; Fig. 13 ; Fig. 14		-	7	-	nC
Q_{GS}	gate-source charge	$I_D = 4.8\ A$; $V_{DS} = 50\ V$; $V_{GS} = 10\ V$; $T_j = 25\ ^\circ C$; Fig. 13 ; Fig. 14		-	2.5	-	nC
Q_{GD}	gate-drain charge			-	1.5	-	nC
C_{iss}	input capacitance	$V_{DS} = 50\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$; $T_j = 25\ ^\circ C$; Fig. 15		-	881	-	pF
C_{oss}	output capacitance			-	168	-	pF
C_{rss}	reverse transfer capacitance			-	6	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\ V$; $R_L = 10.4\ \Omega$; $V_{GS} = 10\ V$; $R_{G(ext)} = 5\ \Omega$; $T_j = 25\ ^\circ C$		-	3.6	-	ns
t_r	rise time			-	2.3	-	ns
$t_{d(off)}$	turn-off delay time			-	13	-	ns
t_f	fall time			-	6	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 1.7\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 16		-	0.78	1	V
t_{rr}	reverse recovery time	$I_S = 2.5\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$;		-	40	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$		-	25	-	nC

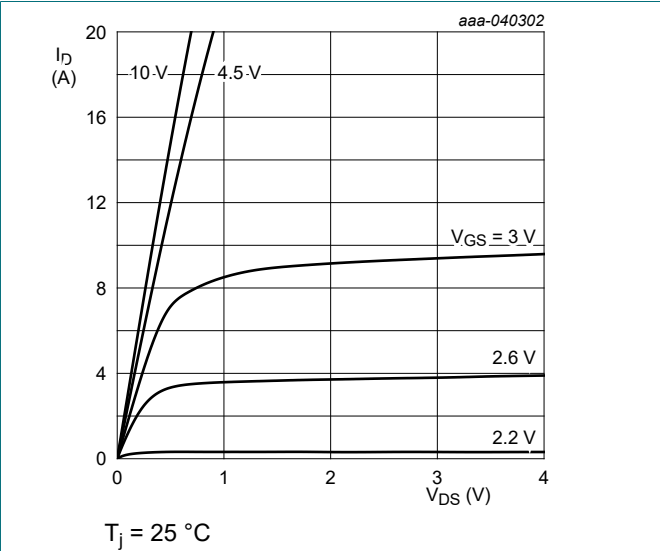


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

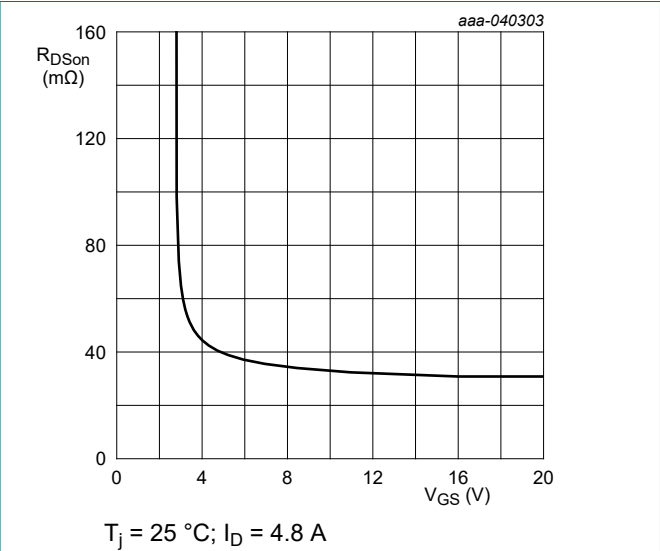


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

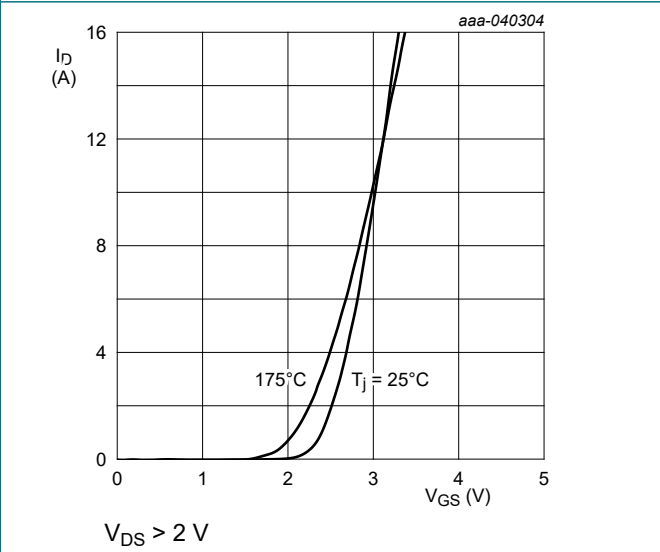


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

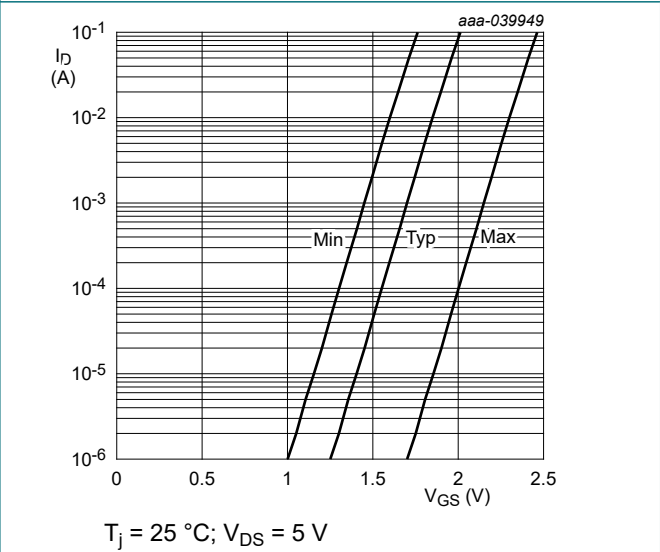


Fig. 9. Sub-threshold drain current as a function of gate-source voltage



Fig. 10. Gate-source threshold voltage as a function of junction temperature

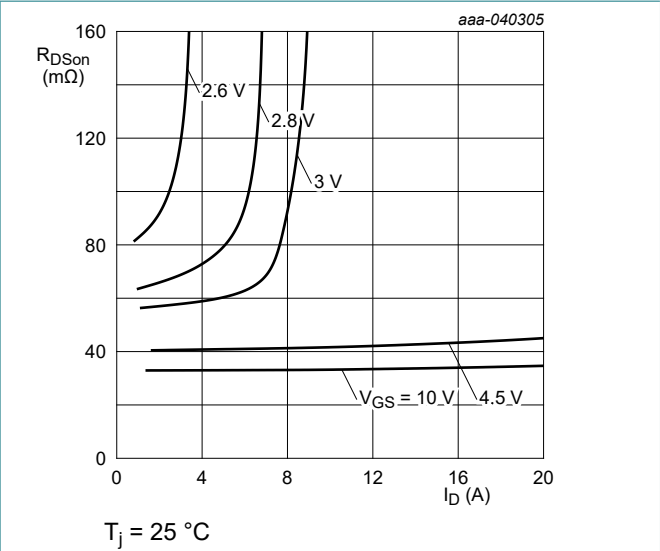


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

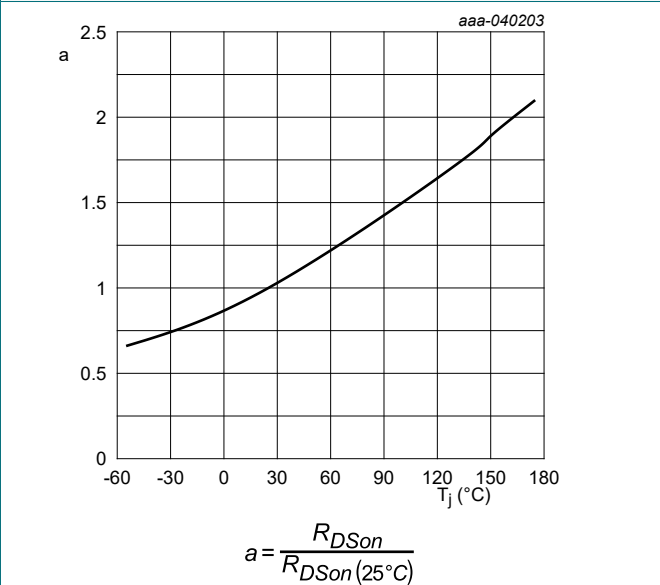


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

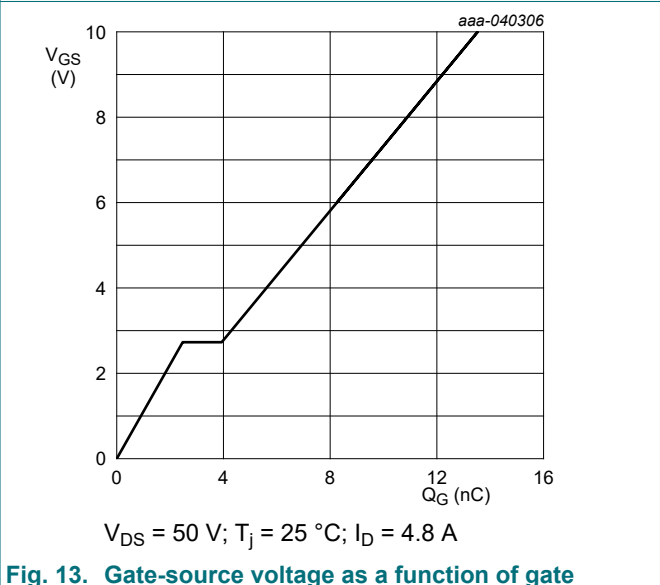


Fig. 13. Gate-source voltage as a function of gate charge; typical values

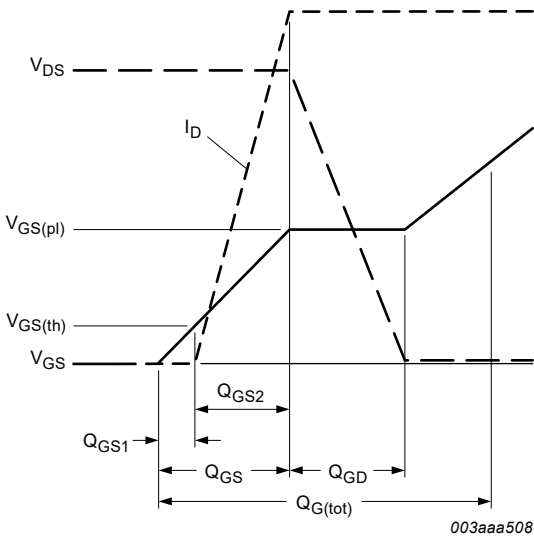


Fig. 14. Gate charge waveform definitions

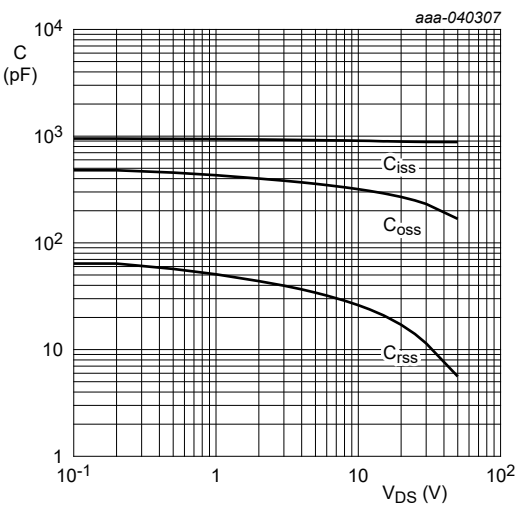
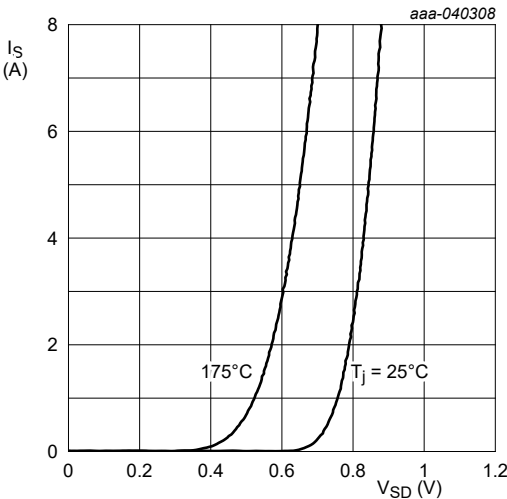


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

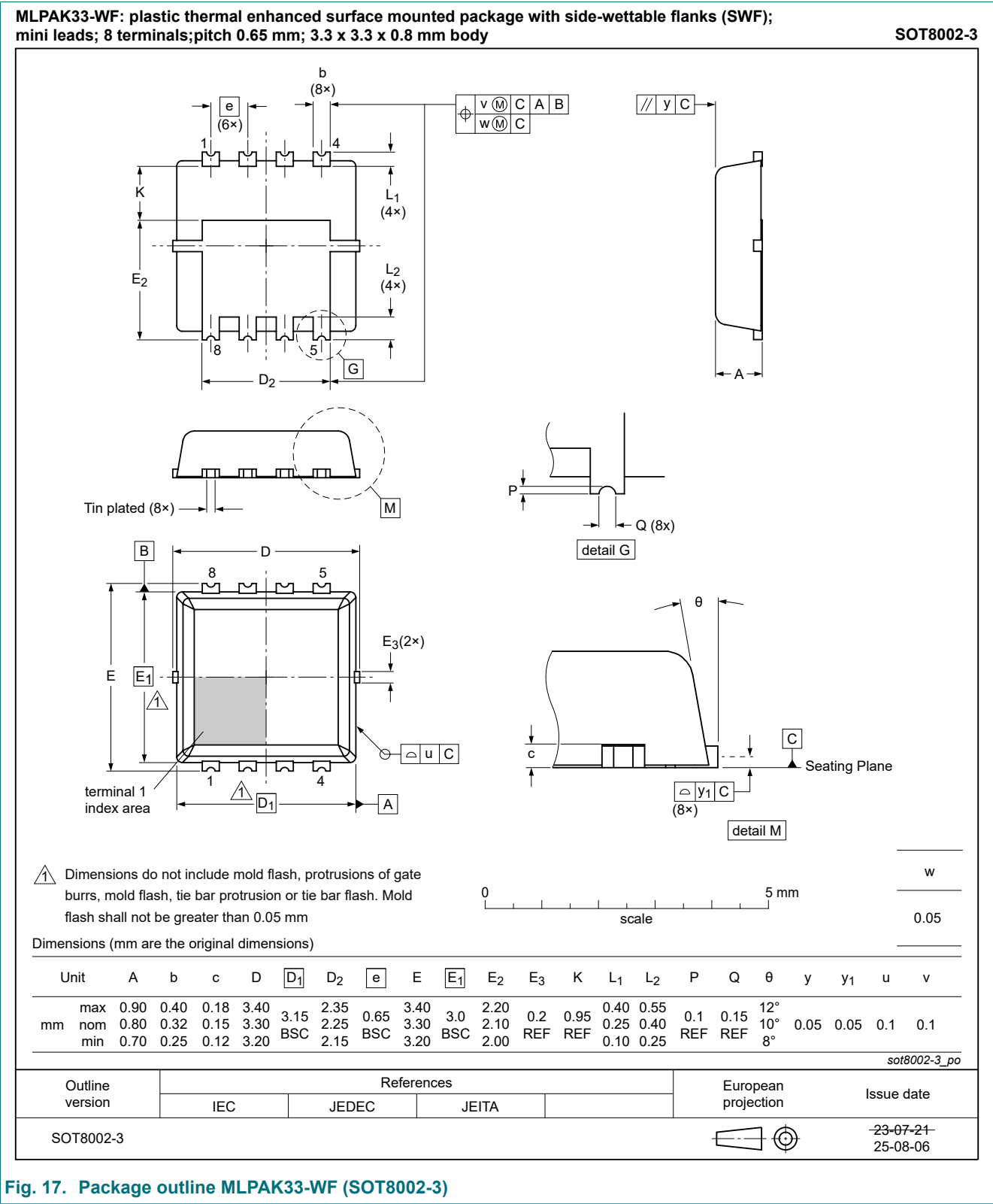


Fig. 17. Package outline MLPAK33-WF (SOT8002-3)

12. Soldering

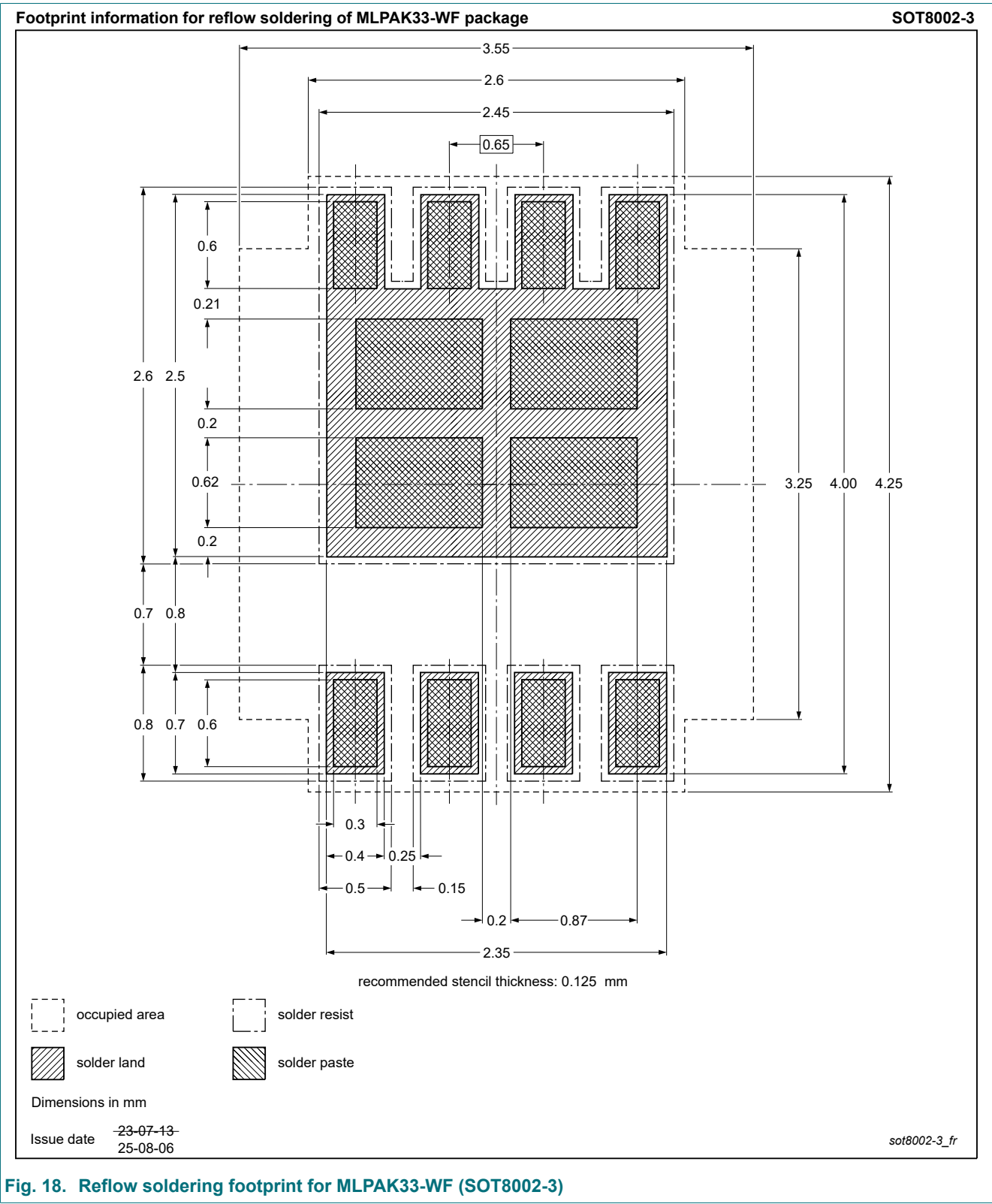


Fig. 18. Reflow soldering footprint for MLPAK33-WF (SOT8002-3)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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