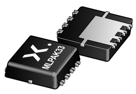


BUK9Q45-80L

80 V, 45 mOhm logic level N-channel MOSFET in MLPAK33

9 December 2025 — Product data sheet

1. General description

Logic level N-channel MOSFET in a small MLPAK33-WF package using Trench12 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Logic-level compatible
- Trench12 MOSFET technology
- Efficient switching with soft body-diode recovery
- Automotive qualified to AEC-Q101 at 175°C
- Side-wettable flanks for robust solder joints and automatic optical inspection

3. Applications

- LED lighting
- DC-to-DC conversion
- Solenoid, motor and other load switching
- Circuit protection

4. Quick reference data

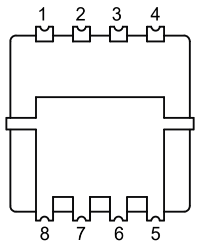
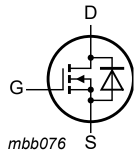
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	80	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	17	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	27.3	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 4.7 A; T_j = 25 °C; Fig. 11		-	35	45	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 4.7 A; V_{DS} = 40 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		-	1.4	-	nC
Source-drain diode							
Q_r	recovered charge	I_S = 1.8 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V; T_j = 25 °C		-	9	-	nC

[1] 17 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **MLPAK33-WF (SOT8002-3)**	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Q45-80L	MLPAK33-WF	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Q45-80L	7AJ

8. Limiting values

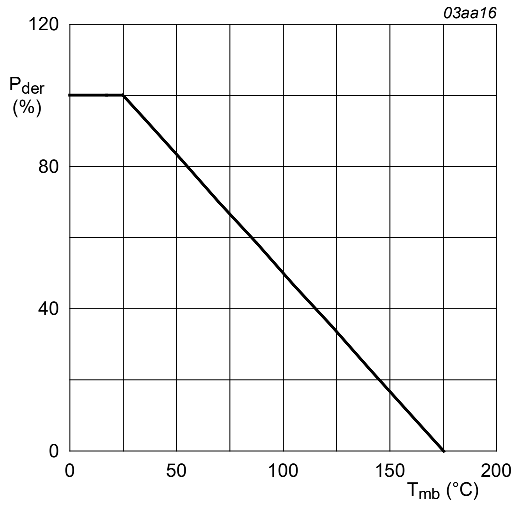
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	27.3	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	17	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	12	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	68	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	17	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	68	A

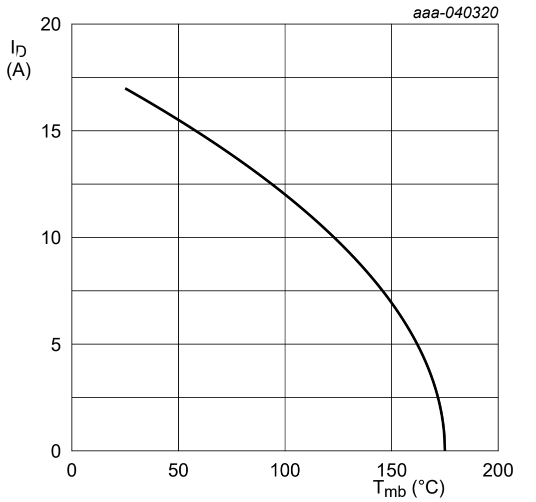
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 6.8 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 65 µs; Fig. 4	[2] [3]	-	23.1	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 80 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[2] [3]	-	6.8	A

[1] 17 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.



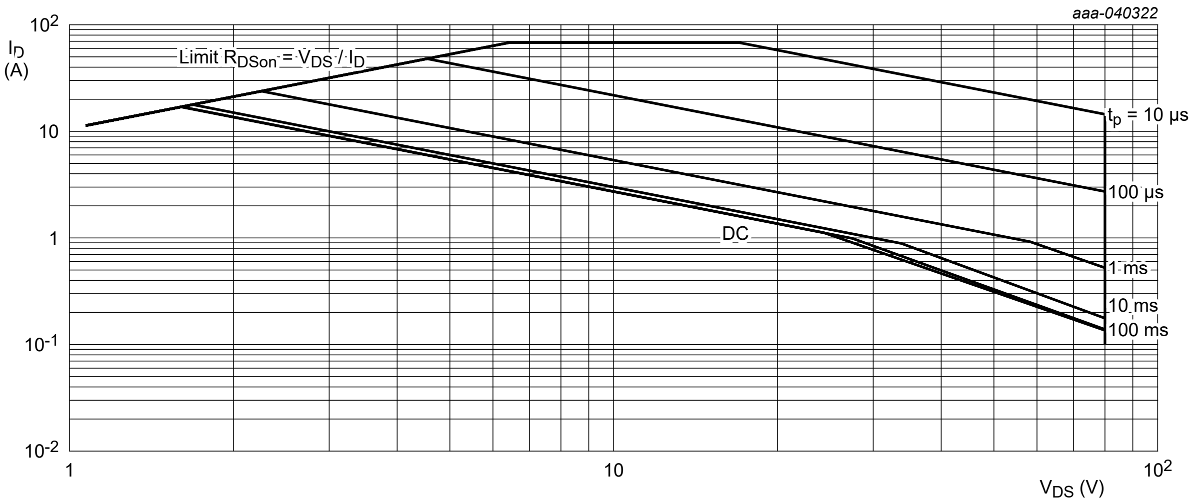
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



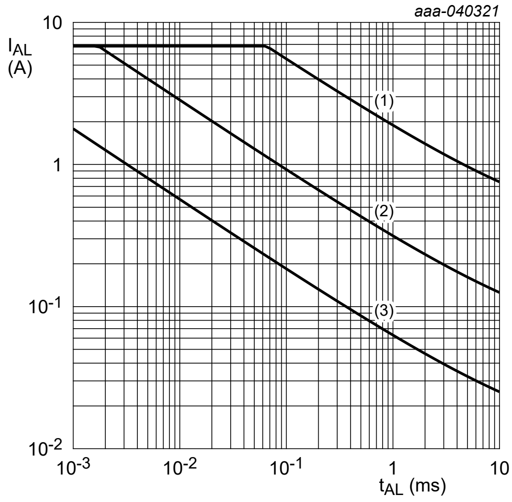
V_{GS} ≥ 10 V

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\,(init)}$ = 25 °C; (2) $T_{j\,(init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	3.7	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	40	-	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.

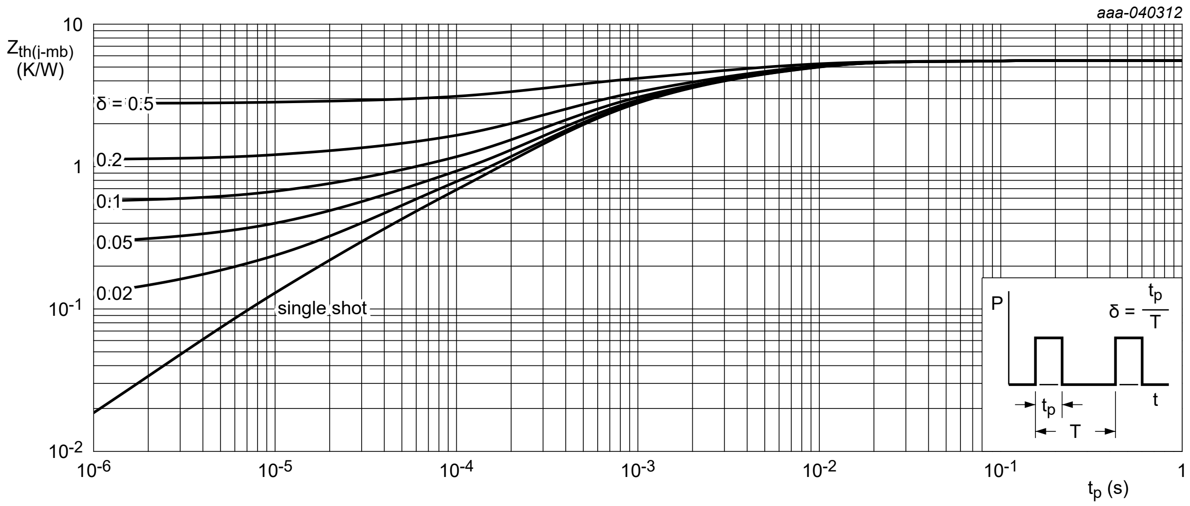


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

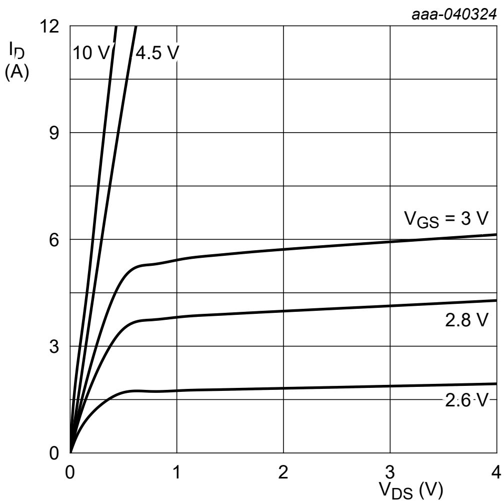
10. Characteristics

Table 7. Characteristics

Tj = 25 °C unless otherwise specified.

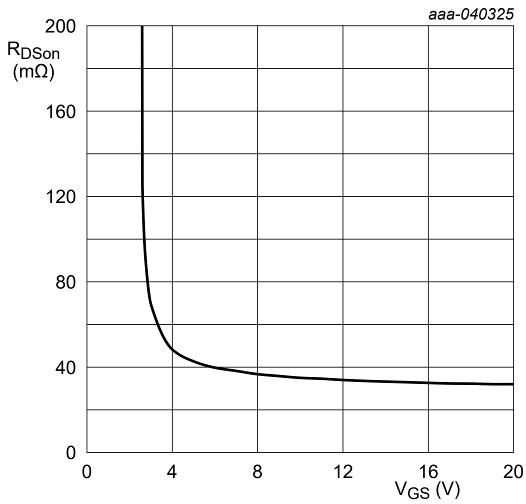
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		80	89	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		77	86	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		76	85	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		1.45	1.7	2.15	V
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 °C		-	-	20	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 175 °C		-	-	200	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 4.7 A; T_j = 25 °C; Fig. 11		-	35	45	mΩ
		V_{GS} = 10 V; I_D = 4.7 A; T_j = 105 °C; Fig. 12		-	54	70	mΩ
		V_{GS} = 10 V; I_D = 4.7 A; T_j = 125 °C; Fig. 12		-	59	77	mΩ
		V_{GS} = 10 V; I_D = 4.7 A; T_j = 175 °C; Fig. 12		-	74	95	mΩ
		V_{GS} = 4.5 V; I_D = 4 A; T_j = 25 °C; Fig. 11		-	46	62	mΩ
		V_{GS} = 4.5 V; I_D = 4 A; T_j = 105 °C; Fig. 12		-	71	99	mΩ
		V_{GS} = 4.5 V; I_D = 4 A; T_j = 125 °C; Fig. 12		-	75	106	mΩ
		V_{GS} = 4.5 V; I_D = 4 A; T_j = 175 °C; Fig. 12		-	93	130	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		-	1.3	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 4.7 A; V_{DS} = 40 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		-	12	18	nC
		I_D = 4.7 A; V_{DS} = 40 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 13; Fig. 14		-	6	-	nC
Q_{GS}	gate-source charge	I_D = 4.7 A; V_{DS} = 40 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		-	2.1	-	nC
Q_{GD}	gate-drain charge			-	1.4	-	nC
C_{iss}	input capacitance	V_{DS} = 40 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 15		-	816	-	pF
C_{oss}	output capacitance			-	140	-	pF
C_{rss}	reverse transfer capacitance			-	6	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 40 V; R_L = 9.1 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	3	-	ns
t_r	rise time			-	3	-	ns
$t_{d(off)}$	turn-off delay time			-	12	-	ns
t_f	fall time			-	3	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 1.7 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16	-	0.79	1	V
t_{rr}	reverse recovery time	I_S = 1.8 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V; T_j = 25 °C	-	19	-	ns
Q_r	recovered charge		-	9	-	nC



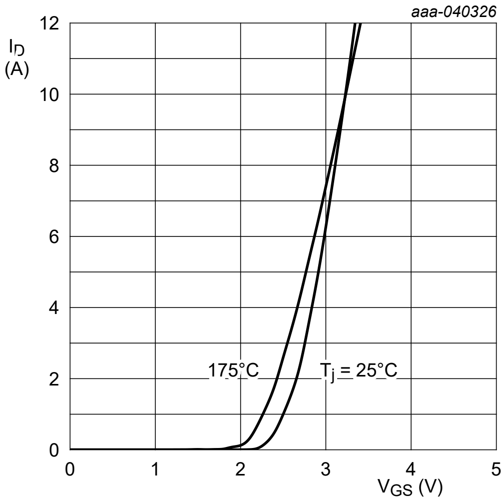
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



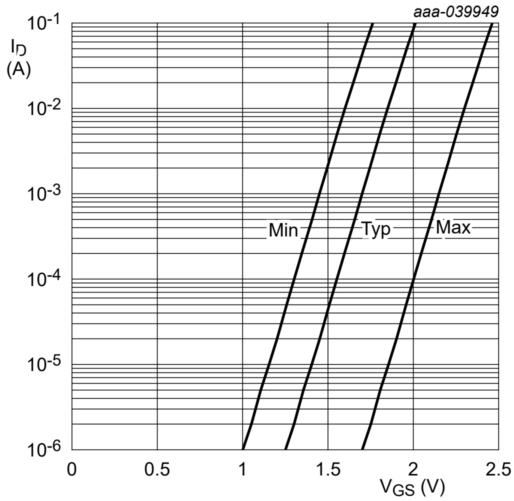
T_j = 25 °C; I_D = 4.7 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



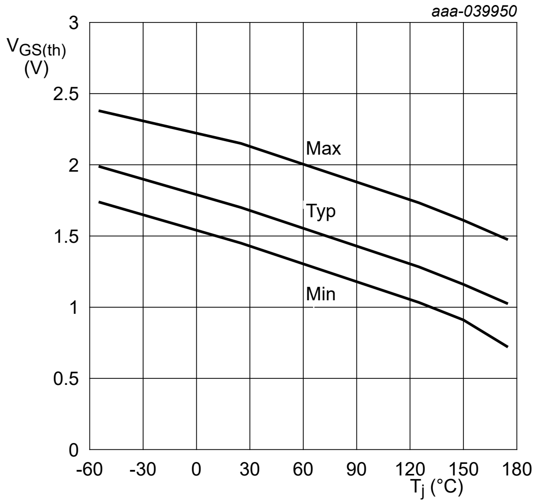
V_{DS} > 2 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



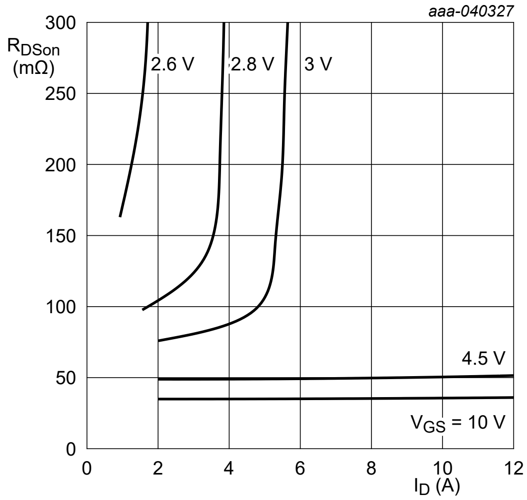
T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold drain current as a function of gate-source voltage



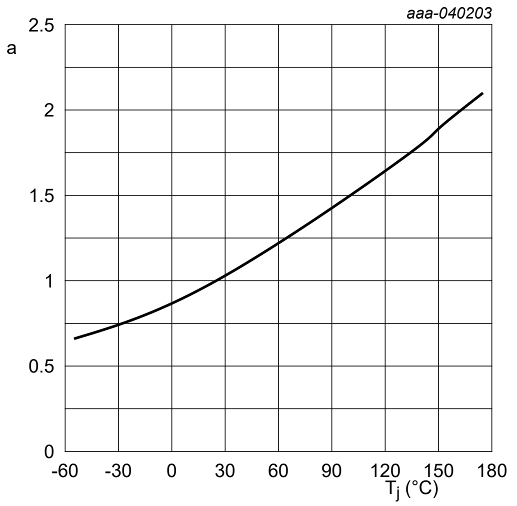
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 10. Gate-source threshold voltage as a function of junction temperature



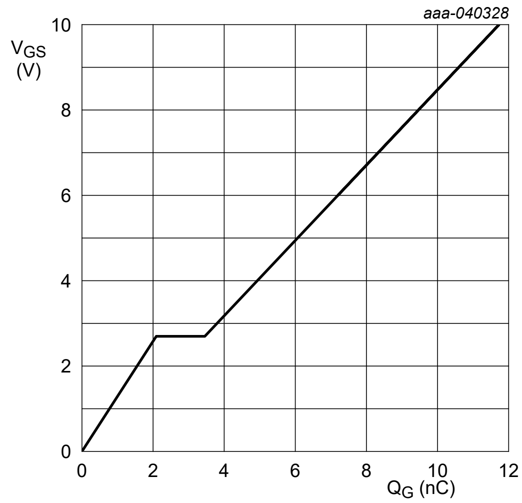
T_j = 25 °C

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



V_{DS} = 40 V; T_j = 25 °C; I_D = 4.7 A

Fig. 13. Gate-source voltage as a function of gate charge; typical values

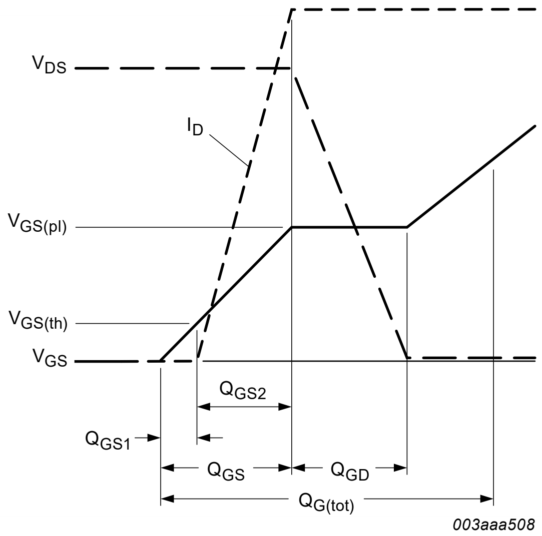
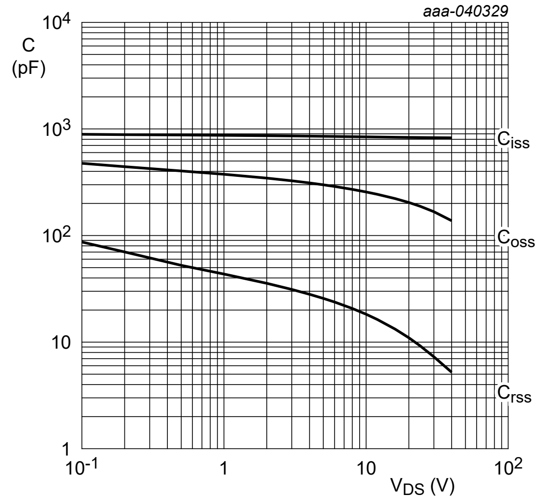
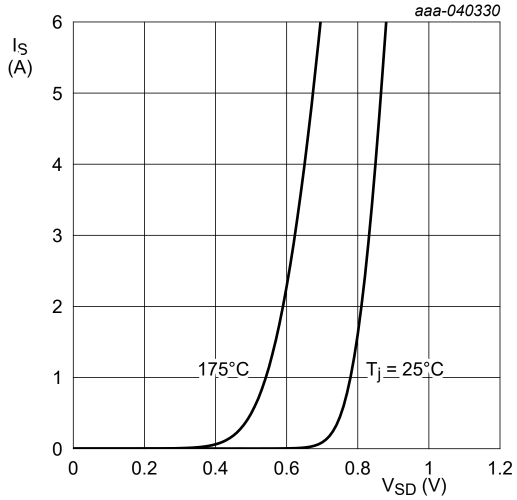


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

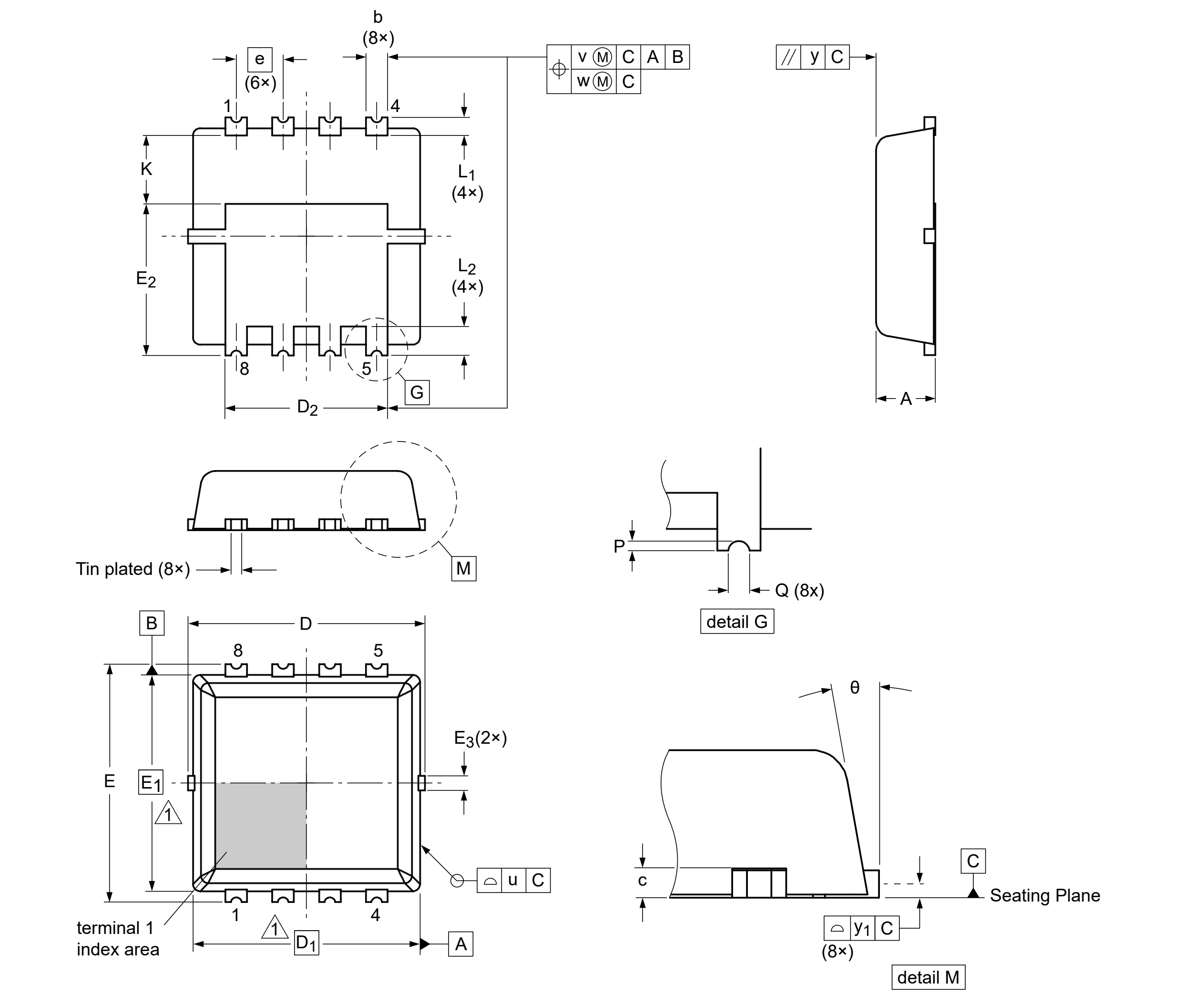


V_{GS} = 0 V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

MLPAK33-WF: plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body **SOT8002-3**



Note 1: Dimensions do not include mold flash, protrusions of gate burrs, mold flash, tie bar protrusion or tie bar flash. Mold flash shall not be greater than 0.05 mm

Dimensions (mm are the original dimensions)

Unit		A	b	c	D	D1	D2	e	E	E1	E2	E3	K	L1	L2	P	Q	θ	y	y1	u	v	w
mm	max	0.90	0.40	0.18	3.40		2.35		3.40		2.20			0.40	0.55			12°					
	nom	0.80	0.32	0.15	3.30	3.15 BSC	2.25	0.65 BSC	3.30	3.0 BSC	2.10	0.2 REF	0.95 REF	0.25	0.40	0.1 REF	0.15 REF	10°	0.05	0.05	0.1	0.1	0.05
	min	0.70	0.25	0.12	3.20		2.15		3.20		2.00			0.10	0.25			8°					

sot8002-3_po

Outline version	References: IEC	JEDEC	JEITA		European projection	Issue date
SOT8002-3						~~23-07-21~~ 25-08-06

Fig. 17. Package outline MLPAK33-WF (SOT8002-3)

12. Soldering

Footprint information for reflow soldering of MLPAK33-WF package **SOT8002-3**

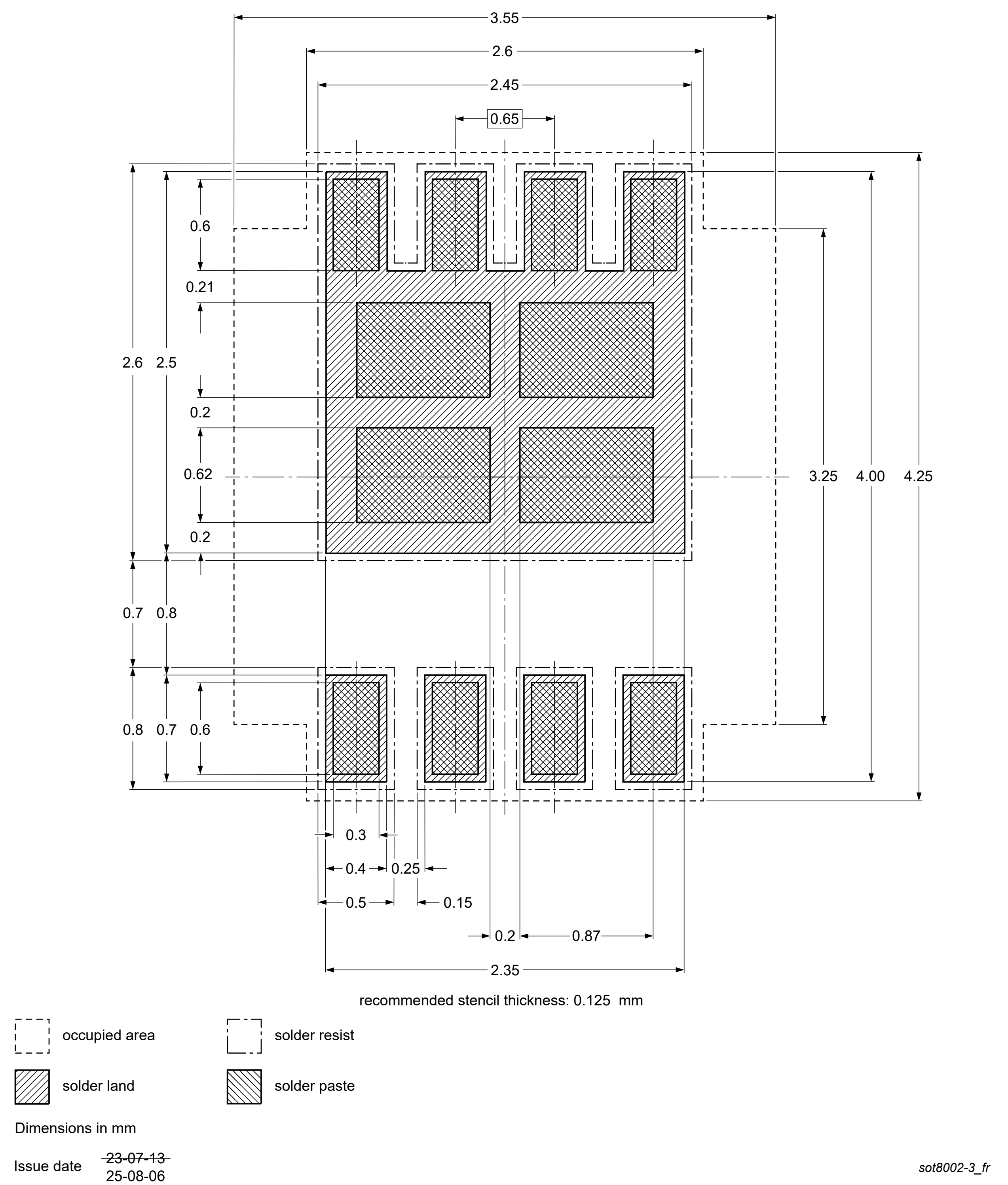


Fig. 18. Reflow soldering footprint for MLPAK33-WF (SOT8002-3)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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