



PDTA124ET-Q

50 V, 100 mA PNP resistor-equipped transistor;
R1 = 22 kΩ, R2 = 22 kΩ

8 September 2025

Product data sheet

1. General description

PNP Resistor-Equipped Transistor (RET) in a small SOT23 Surface-Mounted Device (SMD) plastic package.

NPN complement: PDTC124ET-Q

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Digital application in automotive and industrial segments
- Cost-saving alternative for BC847 series in digital applications
- Controlling IC inputs
- Switching loads

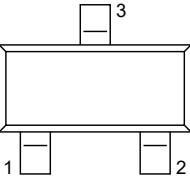
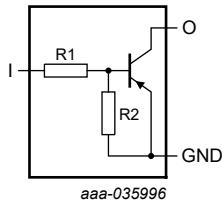
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base		-	-	-50	V
I _O	output current			-	-	-100	mA
R ₁	bias resistor 1 (input)			15.4	22	28.6	kΩ
R ₂ /R ₁	bias resistor ratio			0.8	1	1.2	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 SOT23	 aaa-035996
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTA124ET-Q	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PDTA124ET-Q	%05

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	-50	V
V_{CEO}	collector-emitter voltage	open base		-	-50	V
V_{EBO}	emitter-base voltage	open collector		-	-10	V
V_I	input voltage	positive		-	10	V
		negative		-	-40	V
I_O	output current			-	-100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25^\circ\text{C}$	[1]	-	250	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.

50 V, 100 mA PNP resistor-equipped transistor; R1 = 22 kΩ, R2 = 22 kΩ

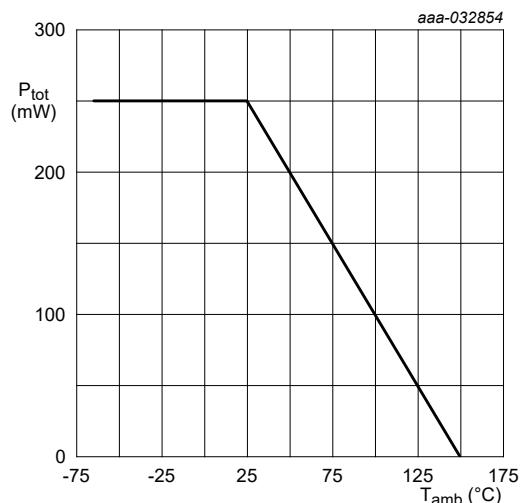


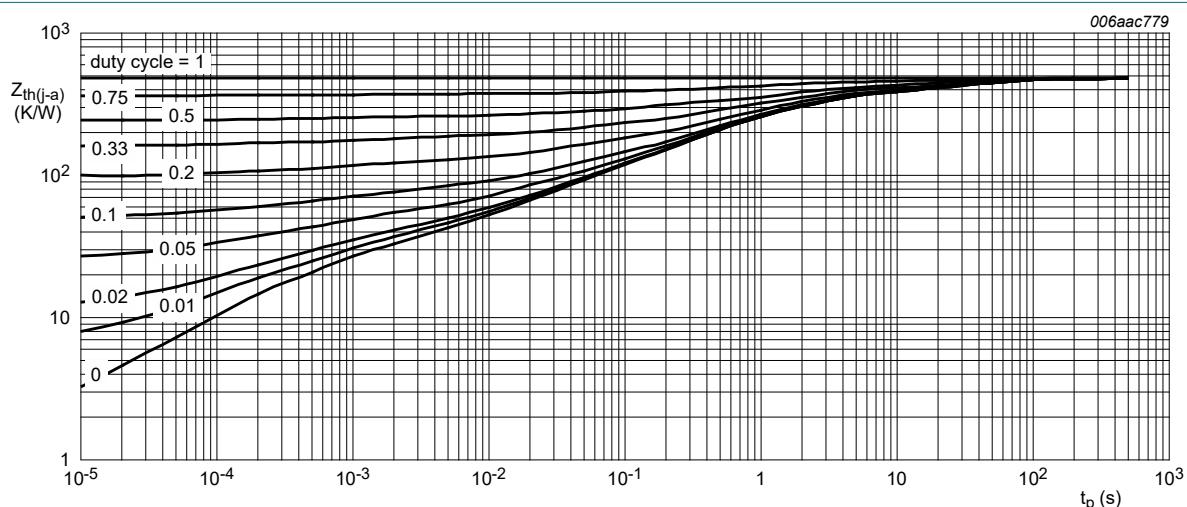
Fig. 1. Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.

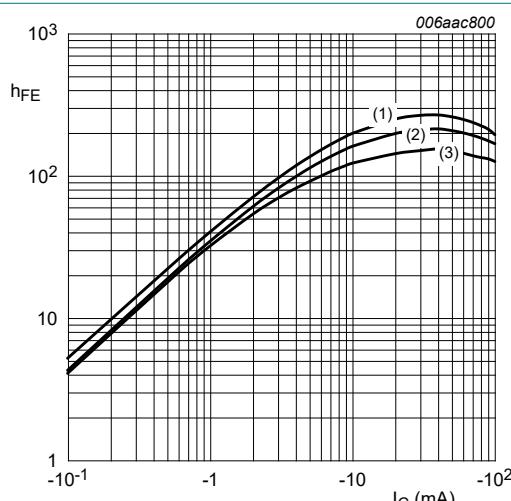
Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

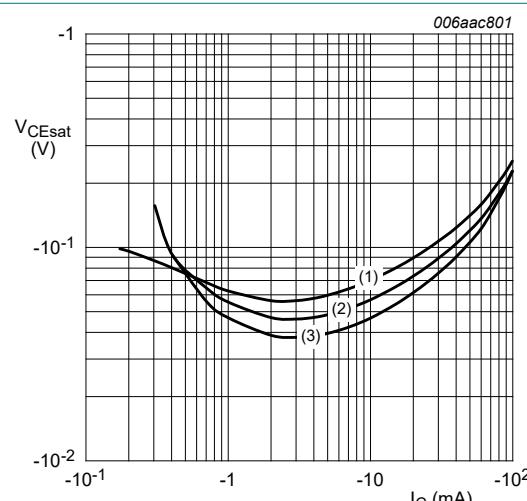
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = -100 \mu A; I_E = 0 A; T_{amb} = 25^\circ C$	-50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = -2 mA; I_B = 0 A; T_{amb} = 25^\circ C$	-50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = -50 V; I_E = 0 A; T_{amb} = 25^\circ C$	-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30 V; I_B = 0 A; T_{amb} = 25^\circ C$	-	-	-100	nA
		$V_{CE} = -30 V; I_B = 0 A; T_j = 150^\circ C$	-	-	-5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5 V; I_C = 0 A; T_{amb} = 25^\circ C$	-	-	-180	μA
h_{FE}	DC current gain	$V_{CE} = -5 V; I_C = -5 mA; T_{amb} = 25^\circ C$	60	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10 mA; I_B = -0.5 mA; T_{amb} = 25^\circ C$	-	-	-150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 V; I_C = -100 \mu A; T_{amb} = 25^\circ C$	-	-1.1	-0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3 V; I_C = -5 mA; T_{amb} = 25^\circ C$	-2.5	-1.7	-	V
R1	bias resistor 1 (input)		15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25^\circ C$	-	-	3	pF
f_T	transition frequency	$V_{CE} = -5 V; I_C = -10 mA; f = 100 MHz; T_{amb} = 25^\circ C$	[1]	-	180	MHz

[1] Characteristics of built-in transistor.



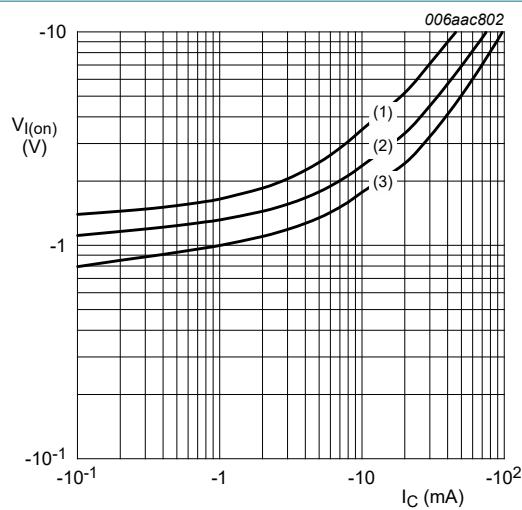
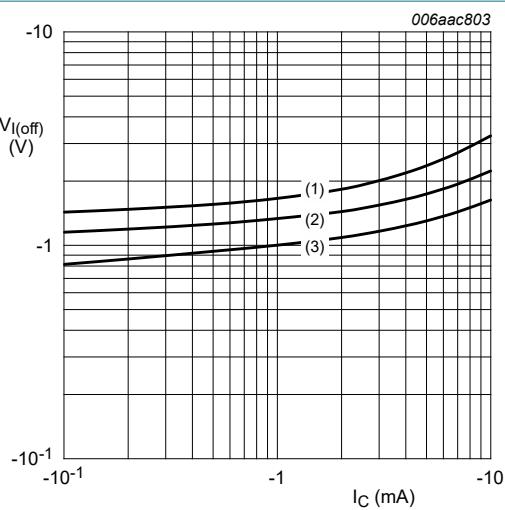
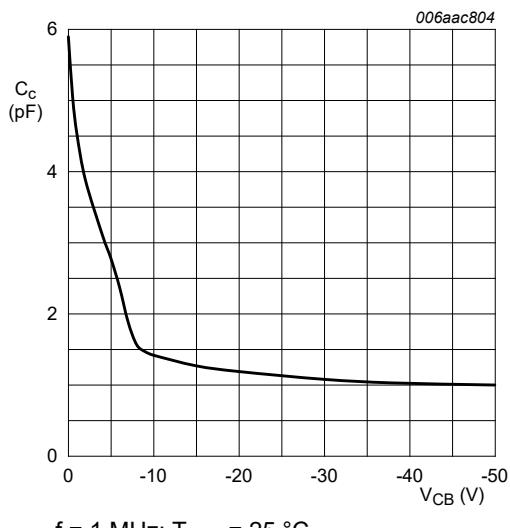
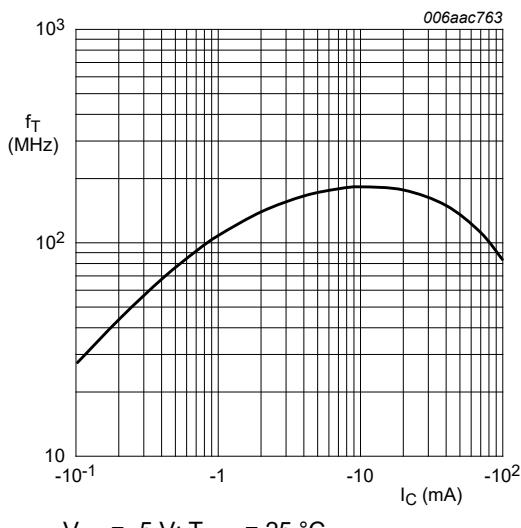
$V_{CE} = -5 V$
 (1) $T_{amb} = 100^\circ C$
 (2) $T_{amb} = 25^\circ C$
 (3) $T_{amb} = -40^\circ C$

Fig. 3. DC current gain as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = 100^\circ C$
 (2) $T_{amb} = 25^\circ C$
 (3) $T_{amb} = -40^\circ C$

Fig. 4. Collector-emitter saturation voltage as a function of collector current; typical values

50 V, 100 mA PNP resistor-equipped transistor; $R1 = 22 \text{ k}\Omega$, $R2 = 22 \text{ k}\Omega$  $V_{CE} = -0.3 \text{ V}$ (1) $T_{amb} = -40 \text{ }^{\circ}\text{C}$ (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$ (3) $T_{amb} = 100 \text{ }^{\circ}\text{C}$ **Fig. 5. On-state input voltage as a function of collector current; typical values** $V_{CE} = -5 \text{ V}$ (1) $T_{amb} = -40 \text{ }^{\circ}\text{C}$ (2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$ (3) $T_{amb} = 100 \text{ }^{\circ}\text{C}$ **Fig. 6. Off-state input voltage as a function of collector current; typical values** $f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^{\circ}\text{C}$ **Fig. 7. Collector capacitance as a function of collector-base voltage; typical values** $V_{CE} = -5 \text{ V}; T_{amb} = 25 \text{ }^{\circ}\text{C}$ **Fig. 8. PNP transistor: Transition frequency as a function of collector current; typical values of built-in transistor**

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

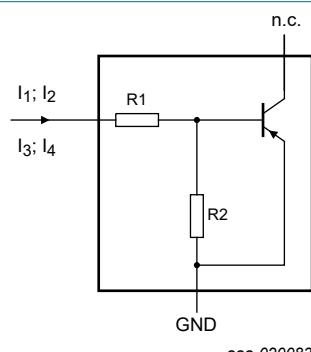


Fig. 9. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
PDTA124ET-Q	22	22	-150 µA	-230 µA	150 µA	230 µA

12. Package outline

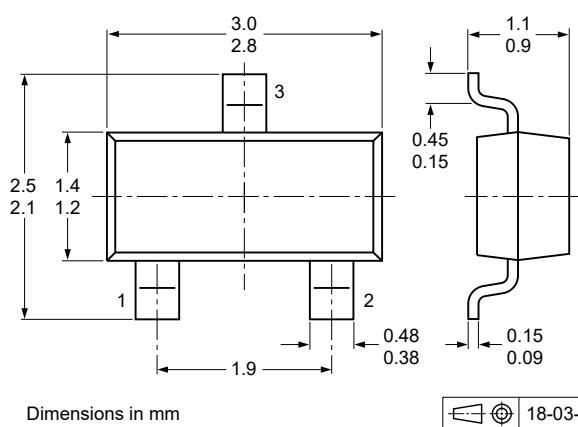


Fig. 10. Package outline SOT23

13. Soldering

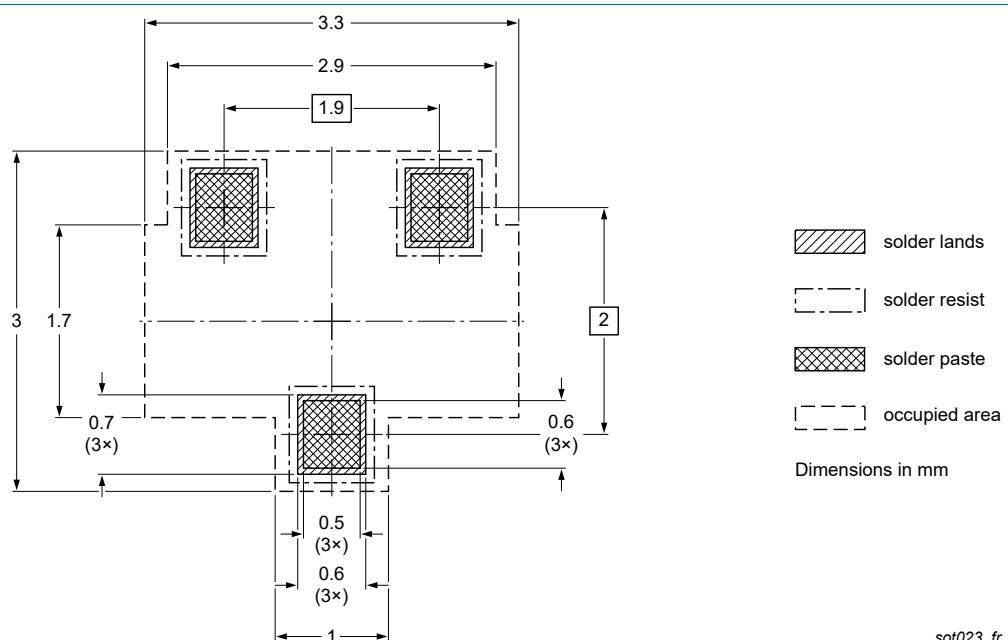


Fig. 11. Reflow soldering footprint for SOT23

50 V, 100 mA PNP resistor-equipped transistor; R1 = 22 kΩ, R2 = 22 kΩ

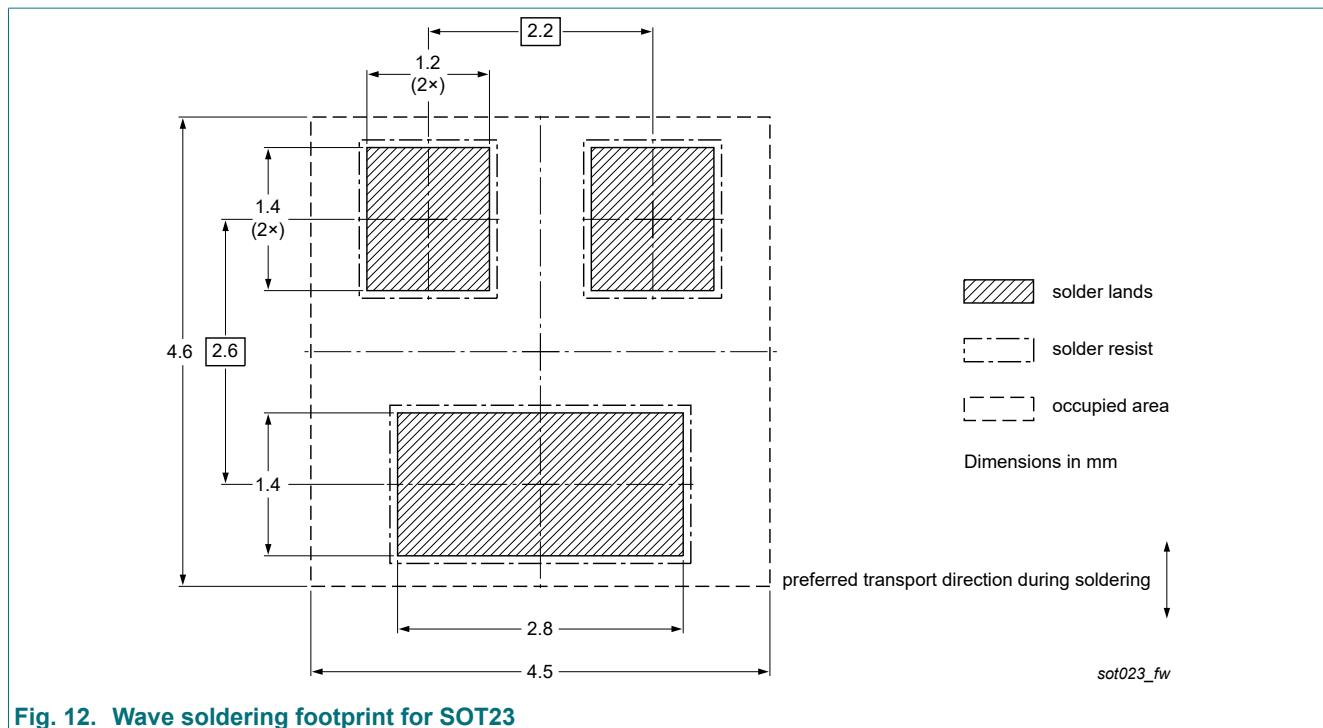


Fig. 12. Wave soldering footprint for SOT23

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTA124ET-Q v.2	20250908	Product data sheet	-	PDTA124ET-Q v.1
Modifications:	<ul style="list-style-type: none">Test information extended			
PDTA124ET-Q v.1	20230111	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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