



# PRMD10

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

25 August 2025

Product data sheet

## 1. General description

NPN/PNP Resistor-Equipped double Transistors (RET) in an ultra small DFN1412-6 (SOT1268) leadless Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PRMH10.

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- AEC-Q101 qualified

## 3. Applications

- Digital applications
- Cost-saving alternative to BC847/BC857 series in digital applications
- Control of IC inputs
- Switching loads

## 4. Quick reference data

Table 1. Quick reference data

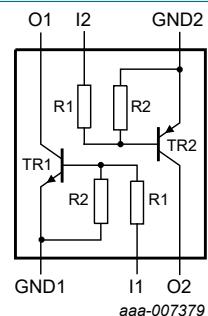
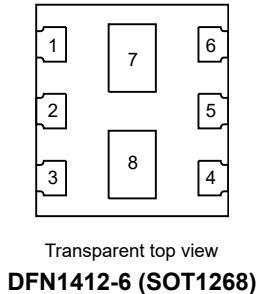
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity							
$V_{CEO}$	collector-emitter voltage	open base		-	-	50	V
$I_O$	output current			-	-	100	mA
$h_{FE}$	DC current gain	$V_{CE} = 5 \text{ V}$ ; $I_C = 10 \text{ mA}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$		100	-	-	
$R1$	bias resistor 1 (input)	$T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	1.54	2.2	2.86	k $\Omega$
$R2/R1$	bias resistor ratio		[1]	17	21	26	

[1] See section "Test information" for resistor calculation and test conditions.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1		
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		



## 6. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description	Version	
PRMD10	DFN1412-6	plastic, thin small outline package; no leads; 6 terminals; 1.4 mm x 1.2 mm x 0.47 mm body		<a href="#">SOT1268</a>

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PRMD10	B5

## 8. Limiting values

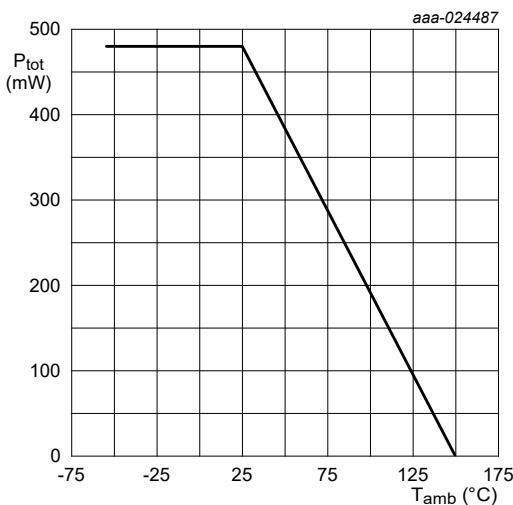
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor, for the PNP transistor with negative polarity</b>						
$V_{CBO}$	collector-base voltage	open emitter		-	50	V
$V_{CEO}$	collector-emitter voltage	open base		-	50	V
$V_{EBO}$	emitter-base voltage	open collector		-	5	V
$V_I$	input voltage	positive		-	12	V
		negative		-	-5	V
$I_O$	output current			-	100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25^\circ\text{C}$	[1]	-	325	mW
<b>Per device</b>						
$P_{tot}$	total power dissipation	$T_{amb} \leq 25^\circ\text{C}$	[1]	-	480	mW
$T_j$	junction temperature			-	150	°C
$T_{amb}$	ambient temperature			-55	150	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

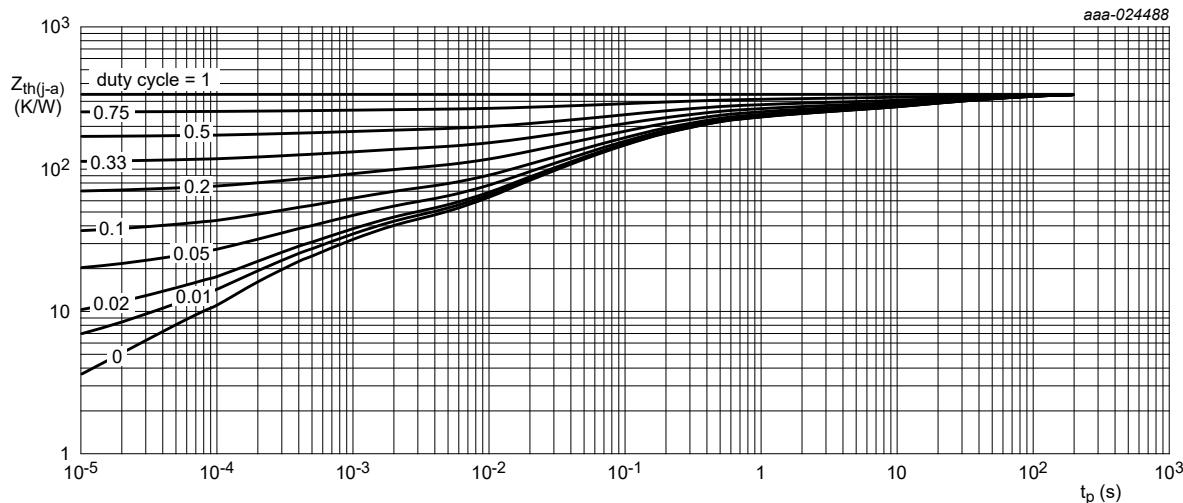
Fig. 1. Per device: Power derating curve

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
<b>Per device</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	261	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

**Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 10. Characteristics

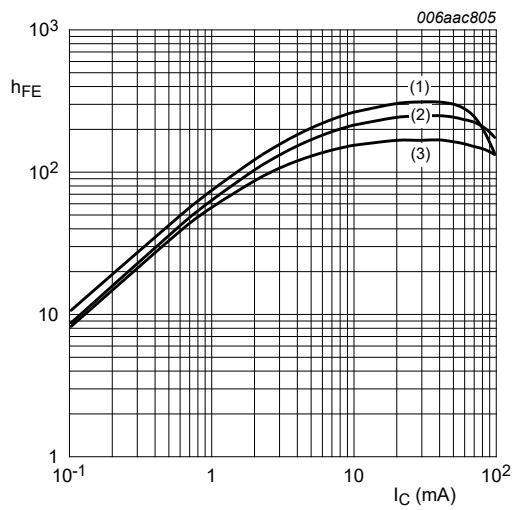
**Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor, for the PNP transistor with negative polarity</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$		-	-	100 nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}$ ; $I_B = 0 \text{ A}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$		-	-	100 nA
		$V_{CE} = 30 \text{ V}$ ; $I_B = 0 \text{ A}$ ; $T_{amb} = 150 \text{ }^\circ\text{C}$		-	-	5 $\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5 \text{ V}$ ; $I_C = 0 \text{ A}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$		-	-	180 $\mu\text{A}$
$h_{FE}$	DC current gain	$V_{CE} = 5 \text{ V}$ ; $I_C = 10 \text{ mA}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	100	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 5 \text{ mA}$ ; $I_B = 0.25 \text{ mA}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$		-	-	100 mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}$ ; $I_C = 100 \mu\text{A}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$		-	0.6	0.5 V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3 \text{ V}$ ; $I_C = 5 \text{ mA}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$		1.1	0.75	- V
$R1$	bias resistor 1 (input)	$T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	1.54	2.2	2.86 k $\Omega$
$R2/R1$	bias resistor ratio		[1]	17	21	26
$C_c$	collector capacitance	$V_{CB} = 10 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $i_e = 0 \text{ A}$ ; $f = 1 \text{ MHz}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$		-	-	2.5 pF
		$V_{CB} = -10 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $i_e = 0 \text{ A}$ ; $f = 1 \text{ MHz}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$		-	-	3 pF
$f_T$	transition frequency	$V_{CE} = 5 \text{ V}$ ; $I_C = 10 \text{ mA}$ ; $f = 100 \text{ MHz}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	[2]	-	230	- MHz
		$V_{CE} = -5 \text{ V}$ ; $I_C = -10 \text{ mA}$ ; $f = 100 \text{ MHz}$ ; $T_{amb} = 25 \text{ }^\circ\text{C}$	[2]	-	180	- MHz

[1] See section "Test information" for resistor calculation and test conditions.

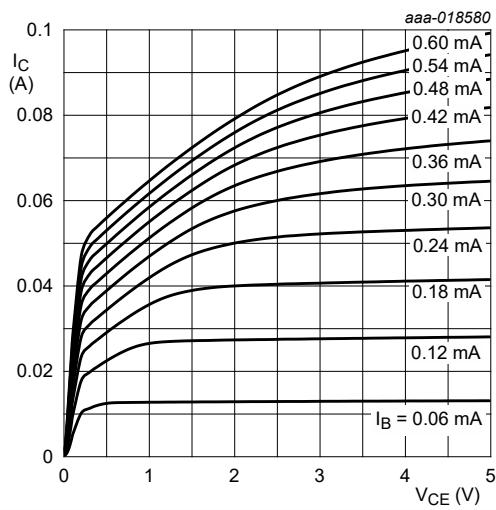
[2] Characteristics of built-in transistor.

## 50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)



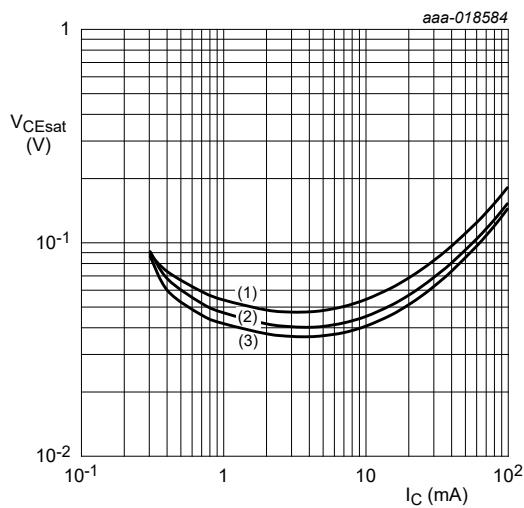
$V_{CE} = 5 \text{ V}$   
 (1)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$

**Fig. 3. NPN transistor: DC current gain as a function of collector current; typical values**



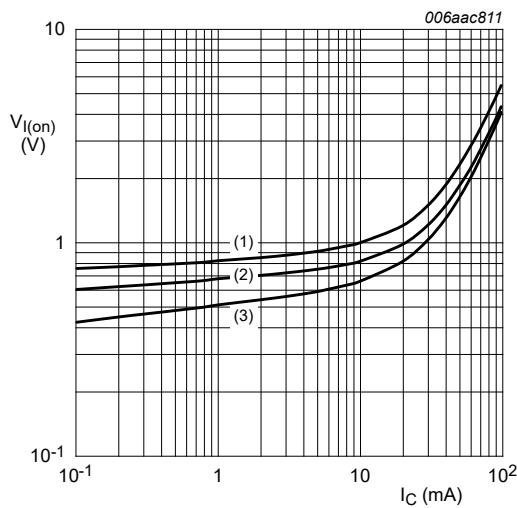
$T_{amb} = 25 \text{ }^{\circ}\text{C}$

**Fig. 4. NPN transistor: Collector current as a function of collector-emitter voltage; typical values**



$I_c/I_b = 20$   
 (1)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$

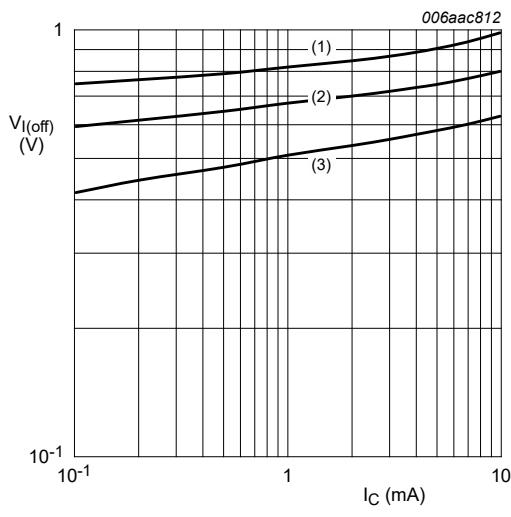
**Fig. 5. NPN transistor: Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = 0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$

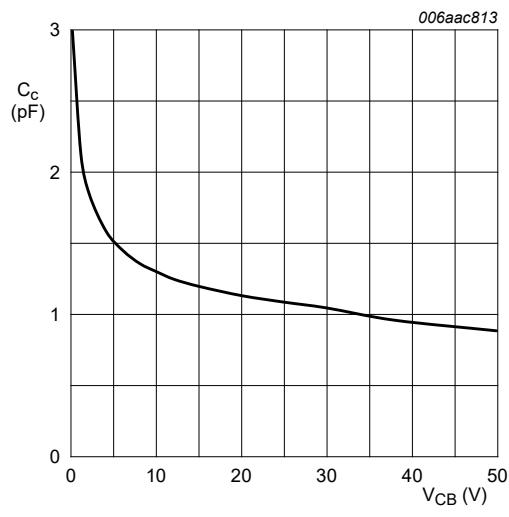
**Fig. 6. NPN transistor: On-state input voltage as a function of collector current; typical values**

## 50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)



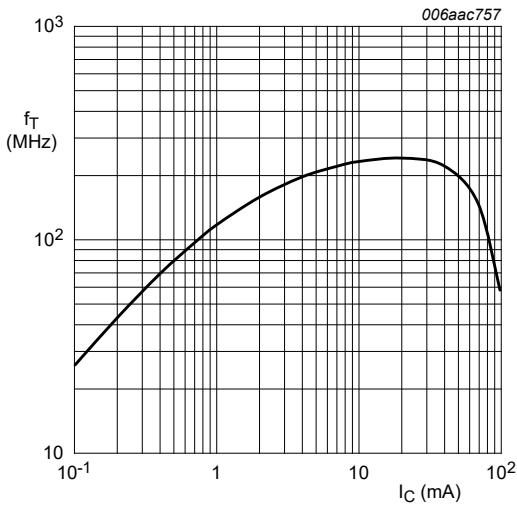
$V_{CE} = 5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$

**Fig. 7. NPN transistor: Off-state input voltage as a function of collector current; typical values**



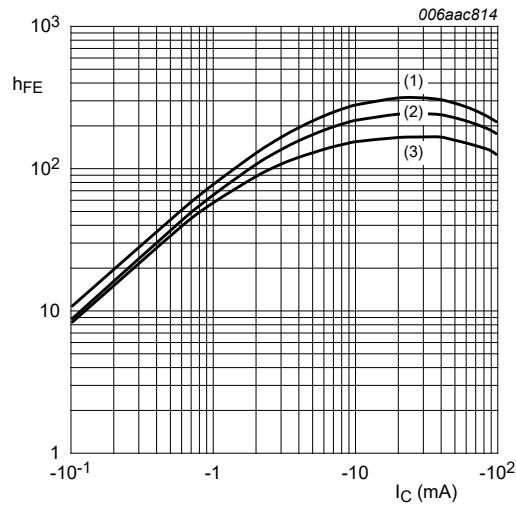
$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^{\circ}\text{C}$

**Fig. 8. NPN transistor: Collector capacitance as a function of collector-base voltage; typical values**



$V_{CE} = 5 \text{ V}; T_{amb} = 25 \text{ }^{\circ}\text{C}$

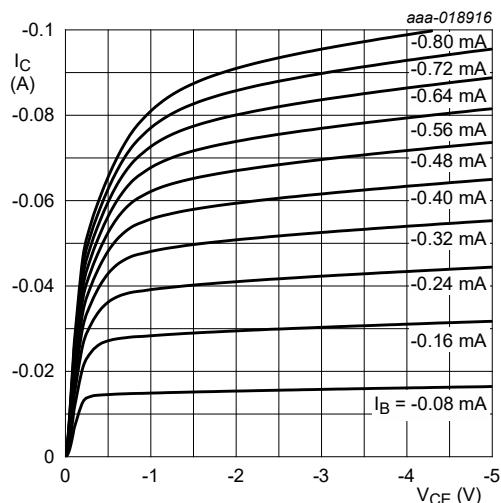
**Fig. 9. NPN transistor: Transition frequency as a function of collector current; typical values of built-in transistor**



$V_{CE} = -5 \text{ V}$   
 (1)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$

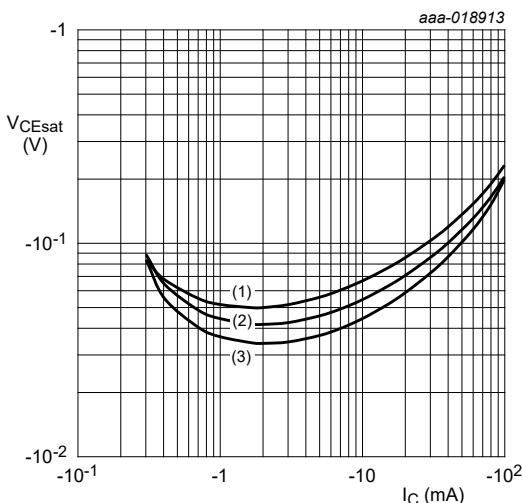
**Fig. 10. PNP transistor: DC current gain as a function of collector current; typical values**

## 50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)



$T_{amb} = 25 \text{ }^{\circ}\text{C}$

**Fig. 11. PNP transistor: Collector current as a function of collector-emitter voltage; typical values**



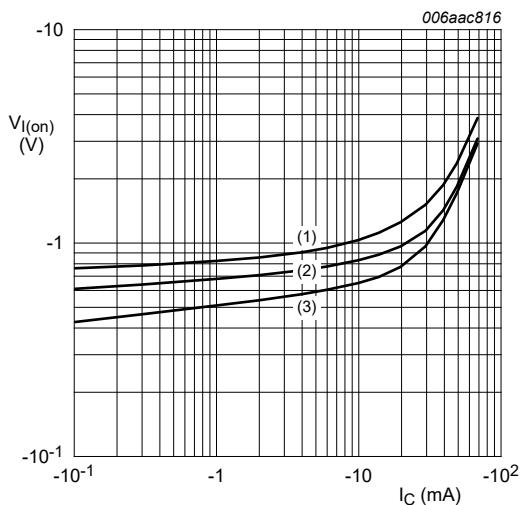
$I_c/I_B = 20$

(1)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$

(2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$

(3)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$

**Fig. 12. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values**



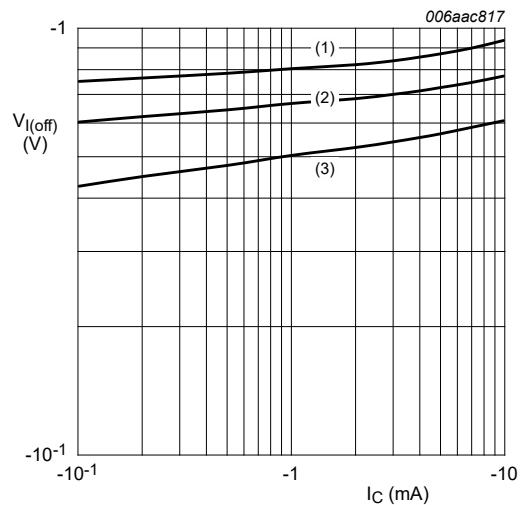
$V_{CE} = -0.3 \text{ V}$

(1)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$

(2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$

(3)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$

**Fig. 13. PNP transistor: On-state input voltage as a function of collector current; typical values**



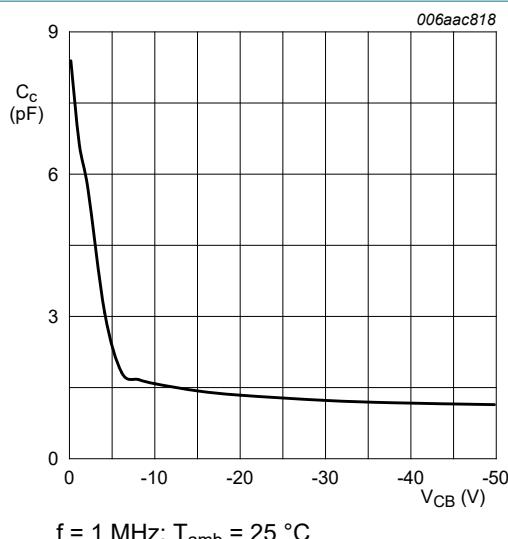
$V_{CE} = -5 \text{ V}$

(1)  $T_{amb} = -40 \text{ }^{\circ}\text{C}$

(2)  $T_{amb} = 25 \text{ }^{\circ}\text{C}$

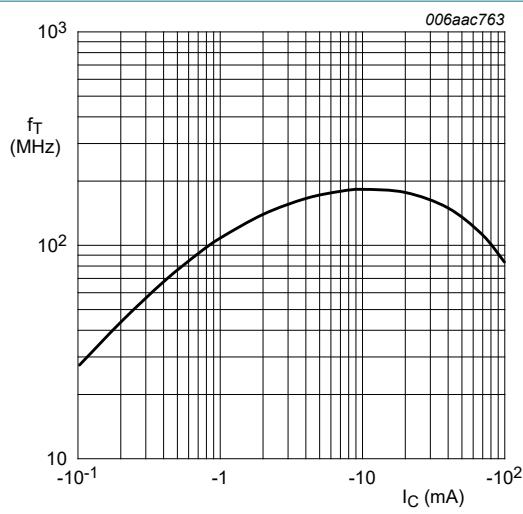
(3)  $T_{amb} = 100 \text{ }^{\circ}\text{C}$

**Fig. 14. PNP transistor: Off-state input voltage as a function of collector current; typical values**



$f = 1$  MHz;  $T_{amb} = 25$  °C

**Fig. 15. PNP transistor: Collector capacitance as a function of collector-base voltage; typical values**



$V_{CE} = -5$  V;  $T_{amb} = 25$  °C

**Fig. 16. PNP transistor: Transition frequency as a function of collector current; typical values of built-in transistor**

## 11. Test information

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

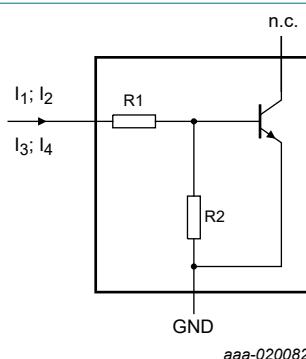
### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$



**Fig. 17. NPN transistor: Resistor test circuit**

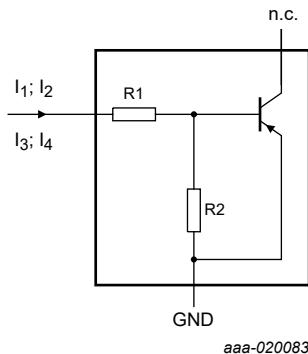


Fig. 18. PNP transistor: Resistor test circuit

### Resistor test conditions

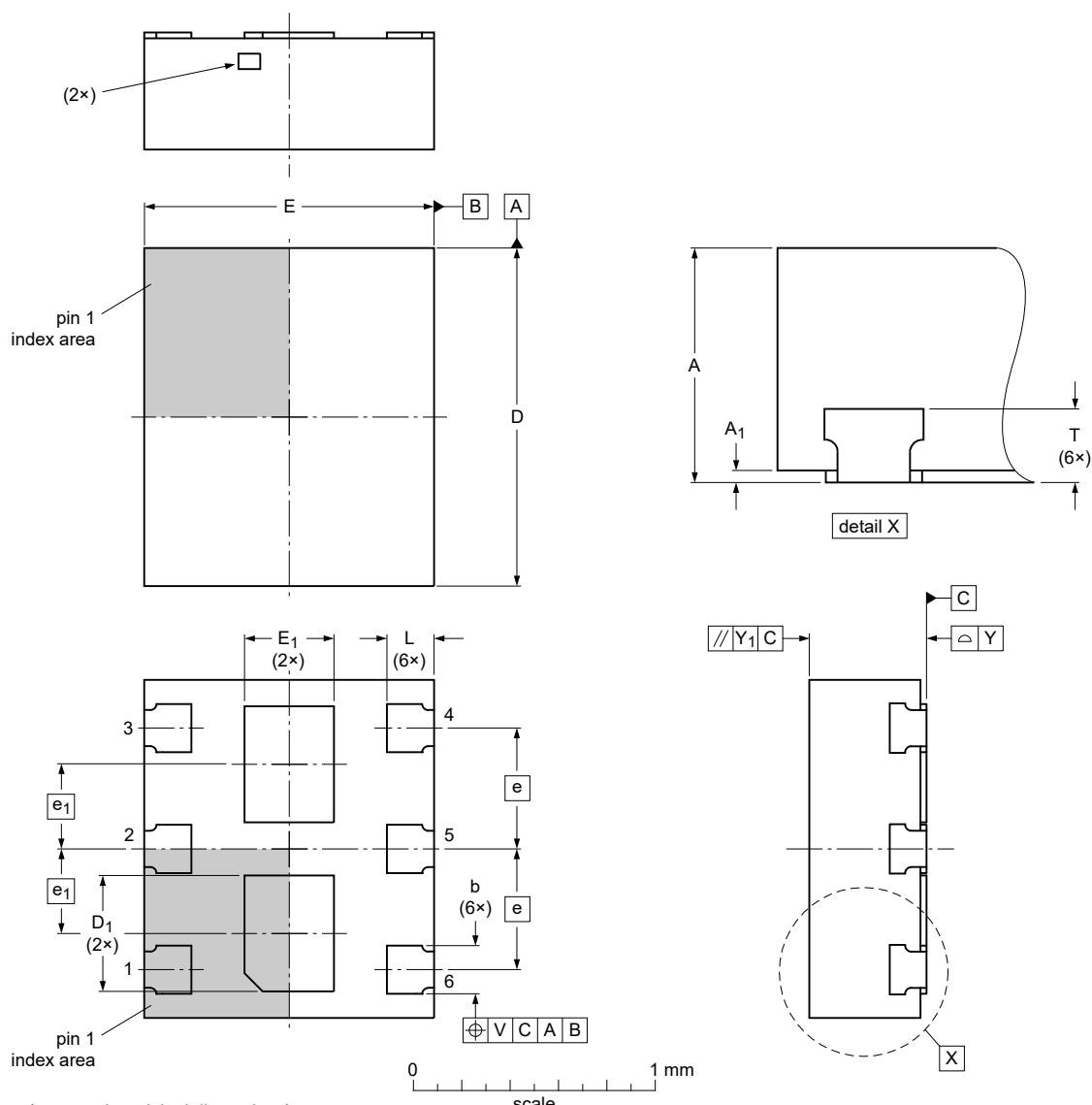
Table 8. Resistor test conditions

Product	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>
TR1 (NPN)	2.2	47	90 µA	140 µA	-55 µA	-105 µA
TR2 (PNP)	2.2	47	-90 µA	-140 µA	55 µA	105 µA

## 12. Package outline

DFN1412-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 x 1.2 x 0.47 mm

SOT1268



Unit <sup>(1)</sup>	A	A <sub>1</sub>	b	D	D <sub>1</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	L	T	V	Y	Y <sub>1</sub>
min	0.44	0.00	0.15	1.35	0.43	1.15	0.32			0.145	0.10			
nom	0.47		0.20	1.40	0.48	1.20	0.37	0.5	0.35	0.195	0.16	0.1	0.05	0.05
max	0.50	0.04	0.25	1.45	0.53	1.25	0.42			0.245	0.22			

Note

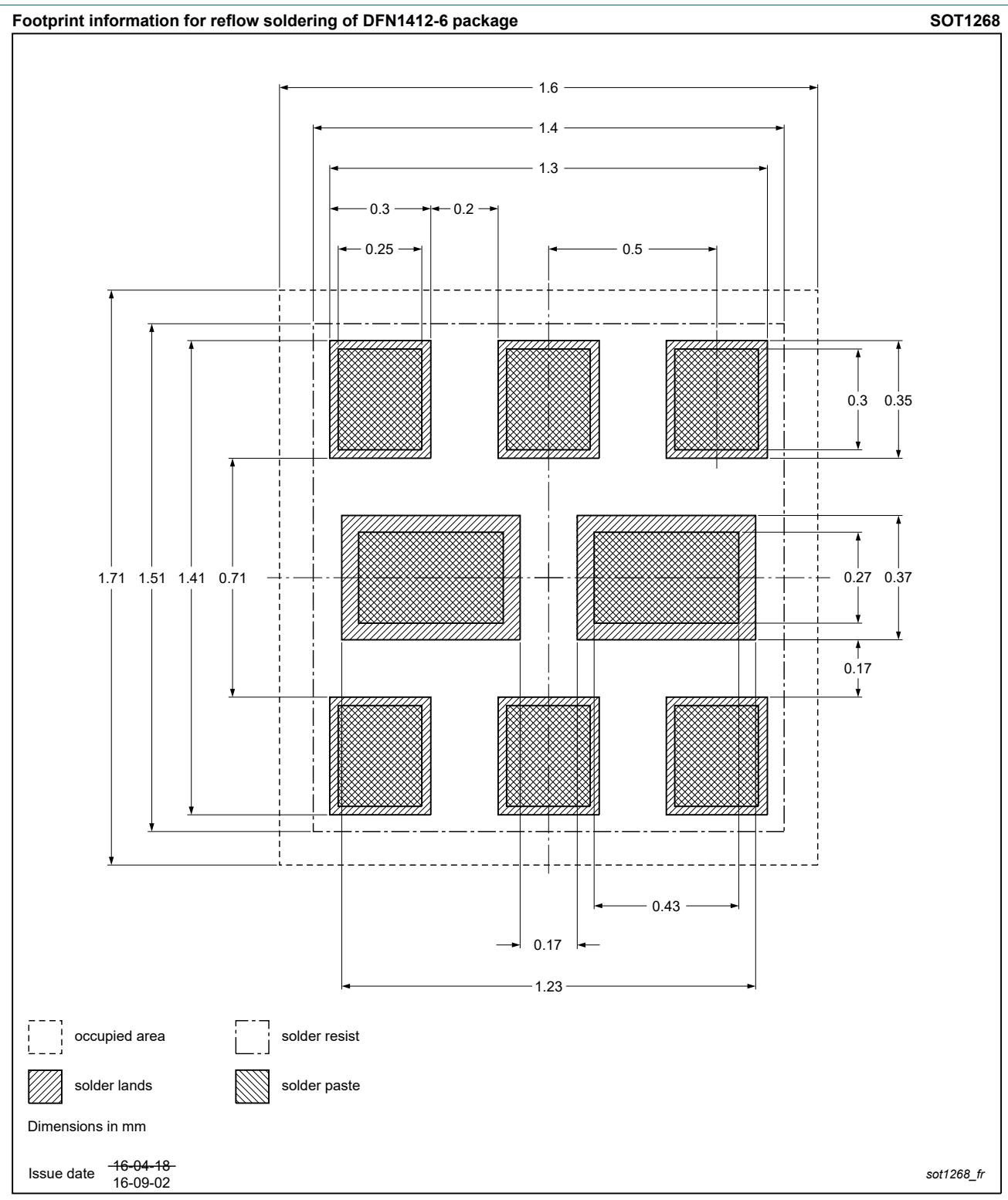
1. Dimension A is including plating thickness.

sot1268\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1268	---				18-08-23 18-09-11

Fig. 19. Package outline DFN1412-6 (SOT1268)

## 13. Soldering



**Fig. 20. Reflow soldering footprint for DFN1412-6 (SOT1268)**

## 14. Revision history

**Table 9. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PRMD10 v.3	2025mmdd	Product data sheet	-	PRMD10 v.2
Modifications:	<ul style="list-style-type: none"><li>Characteristics: Graph 006aac816 of Fig 13 changed</li></ul>			
PRMD10 v.2	20180914	Product data sheet	-	PRMD10 v.1
PRMD10 v.1	20170627	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 25 August 2025

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